RICOH

R3154N-Y Series

42 V Input Window Voltage Detector with Diagnostic Function for Industrial Applications

No. EY-528-200930

OVERVIEW

The R3154N is a Window Voltage Detector suitable for functional safety requirement. This device monitors over-and-under output voltages from the power supply IC for a microprocessor and a sensor, and detects abnormal voltage of systems. Its undervoltage detection down to 0.55 V is suitable for low power devices. Also, operation check of voltage detection is available with the TEST pin. This is a high-reliability semiconductor device for industrial applications (-Y) that has passed both the screening at high temperature and the reliability test with extended hours.

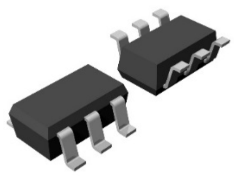
KEY BENEFITS

- Power supply from battery enables the voltage detector to operate independently from the power source.
- High-accuracy over-and-undervoltage detection from -1.25% to 0.75% and the hysteresis of Max. 0.75%.
- Overvoltage detection: 0.75 V at minimum, Undervoltage detection: 0.55 V at minimum.
- Compact package of SOT-23-6. Safe and secure adjacent pin configuration to prevent a short circuit.

KEY SPECIFICATIONS

- Operating Voltage Range (Max. Rating):
  3.0 V to 42.0 V (50.0 V)
- Operating Temperature Range: −40°C to 125°C
- Supply Current: Typ. 2.0 µA
- Overvoltage Detection: 0.75 V to 3.70 V (in 0.01 V step)
  Accuracy (V_{OVSET} > 0.9 V): ±0.5% (Ta = 25°C)
  −1.25% to 0.75% (−40°C to 125°C)
- Undervoltage Detection: 0.55 V to 3.30 V (in 0.01 V step)
  Accuracy (V_{UVSET} > 0.66 V): ±0.5% (Ta = 25°C)
  −1.25% to 0.75% (−40°C to 125°C)
- Detection Release Hysteresis: Typ. 0.5%
- Detection Release Time: Typ. 20 µs
- Release Delay Time: Typ. 4 ms (C_D = 0.01 µF)
- Output Type: Nch. Open Drain

PACKAGE



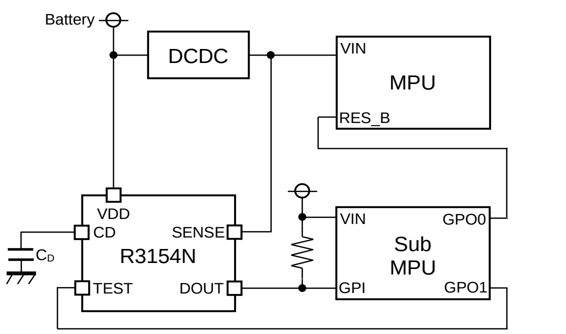
SOT-23-6
2.9 x 2.8 x 1.1 (mm)

SELECTION GUIDE

Product Name	Package	Quantity per Reel
R3154NxxxA-TR-YE	SOT-23-6	3,000 pcs

xxx: The combination of an overvoltage detection setting voltage (V_{OVSET}) and an undervoltage detection setting voltage (V_{UVSET})
Refer to *Product-specific Electrical Characteristics* for details.

TYPICAL APPLICATIONS



C_D: a capacitor corresponding to the set release delay time

APPLICATIONS

- Safety components that require safety standards such as safety light curtains and safety relays.
- FA control equipment and process automation equipment, such as servo amplifiers, safety controllers, PLCs and sequencers with functional safety.

SELECTION GUIDE

The detection setting voltages are user-selectable.

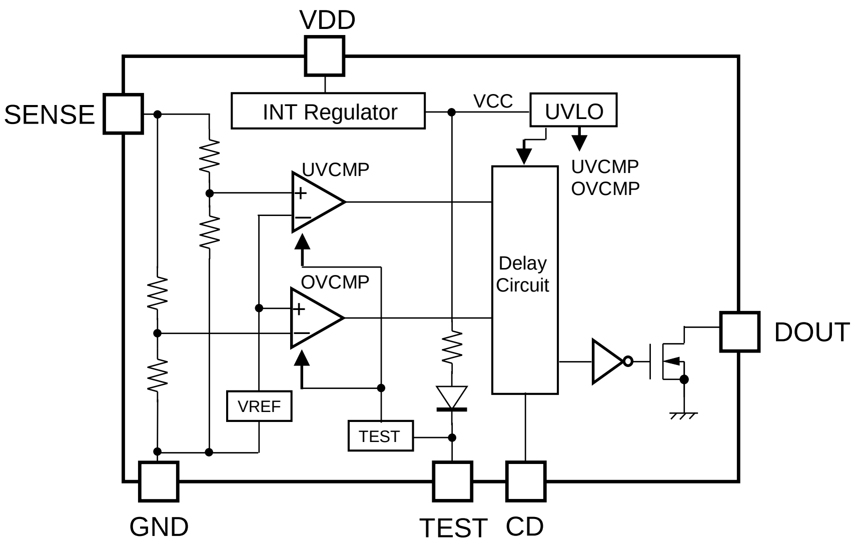
Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3154NxxxA-TR-YE	SOT-23-6	3,000 pcs	Yes	Yes

xxx: The combination of an overvoltage detection setting voltage (V_{OVSET}) and an undervoltage detection setting voltage (V_{UVSET}).

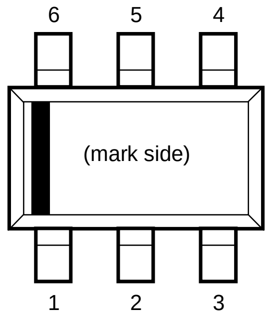
Refer to *Product-specific Electrical Characteristics* for details.

BLOCK DIAGRAM



R3154N Block Diagram

PIN DESCRIPTIONS



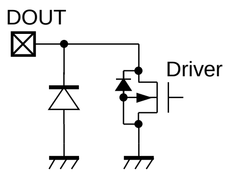
SOT-23-6 Pin Configuration

Pin Descriptions

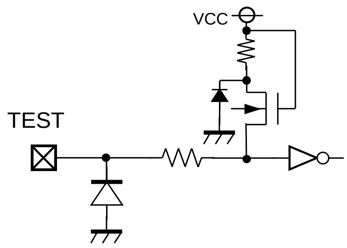
Pin No.	Symbol	Description
1	VDD	Supply Voltage Pin
2	CD	Release Delay Time Set Pin (“Open” when not connected)
3	DOUT	Voltage Fault Detection Output Pin (“Low” at detection)
4	TEST	TEST Pin ("Low" at operation check of voltage detection)
5	GND	GND Pin
6	SENSE	SENSE Voltage Input Pin

Internal Equivalent Circuit for Each Pin

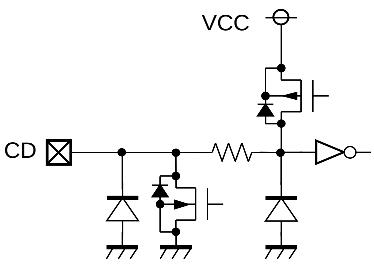
DOUT Pin



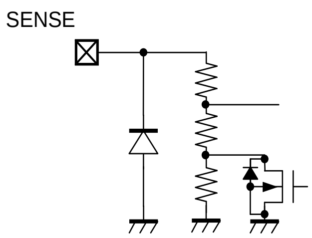
TEST Pin



CD Pin



SENSE Pin



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	−0.3 to 50.0	V
	Peak Voltage[1]	60	V
V_{CD}	CD Pin Output Voltage	−0.3 to 20.0	V
V_{DOUT}	DOUT Pin Output Voltage	−0.3 to 20.0	V
V_{TEST}	TEST Pin Voltage	−0.3 to 20.0	V
V_{SENSE}	SENSE Pin Voltage	−0.3 to 20.0	V
I_{DOUT}	DOUT Pin Output Current	30	mA
P_D	Power Dissipation	Refer to Appendix *"POWER DISSIPATION"*	
Tj	Junction Temperature Range	−40 to 150	°C
Tstg	Storage Temperature Range	−55 to 150	°C

ABSOLUTE MAXIMUM RATINGS
Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	Operating Voltage	3.0 to 42	V
V_{SENSE}	SENSE Input Voltage	0 to 6.0	V
V_{TEST}	TEST Pin Voltage	0 to 6.0	V
V_{UP}	DOUT Pin Pull-up Voltage	0 to 6.0	V
Ta	Operating Temperature Range	−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

[1] Duration Time: Within 200 ms

ELECTRICAL CHARACTERISTICS

V_{DD} = 14 V, C_D = 0.01 µF, pulled-up to 5 V with 100 kΩ, unless otherwise specified.

The specifications surrounded by ☐ are guaranteed by design engineering at -40°C ≤ Ta ≤ 125°C.

R3154N (-YE) Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{OVDET}	Overvoltage (OV) Detector Threshold	Ta = 25°C	0.9 V < V_{OVSET}	x0.995		x1.005	V
			V_{OVSET} ≤ 0.9 V	–4.5		+4.5	mV
		–40°C ≤ Ta ≤ 125°C	0.9 V < V_{OVSET}	x0.9875		x1.0075	V
			V_{OVSET} ≤ 0.9 V	-11.25		+6.75	mV
V_{UVDET}	Undervoltage (UV) Detector Threshold	Ta = 25°C	0.66V < V_{UVSET}	x0.995		x1.005	V
			V_{UVSET} ≤ 0.66V	-3.3		+3.3	mV
		–40°C ≤ Ta ≤ 125°C	0.66 V< V_{UVSET}	x0.9875		x1.0075	V
			V_{UVSET} ≤ 0.66V	-8.25		+4.95	mV
V_{OVHYS}	Overvoltage (OV) Threshold Hysteresis			V_{OVDET} ×0.0025	V_{OVDET} ×0.005	V_{OVDET} ×0.0075	V
V_{UVHYS}	Undervoltage (UV) Threshold Hysteresis			V_{UVDET} ×0.0025	V_{UVDET} ×0.005	V_{UVDET} ×0.0075	V
I_{SS}	Supply Current	V_{UVDET} < V_{SENSE} < V_{OVDET}			2.0	5.0	µA
R_{SENSE}	SENSE Pin Resistance(1)	Resistance between SENSE and GND		3		32	MΩ
V_{UVLO}	UVLO Detector Threshold				1.8	2.7	V
$V_{UVLOHYS}$	UVLO Threshold Hysteresis				0.1	0.3	V
V_{DDL}	DOUT Pin Output Low-operating Voltage(2)					1.7	V
I_{OUT}	NMOS Driver Output Current	V_{DD} = 3.0, V_{DS} = 0.1 V		0.37	0.75		mA
I_{LEAK}	NMOS Driver Leakage Current	V_{DOUT} = 5.5 V			0	1	µA
V_{TESTH}	TEST Pin Input Voltage, "High"			1.6			V
V_{TESTL}	TEST Pin Input Voltage, "Low"					0.5	V
t_{DELAY}	Release Delay Time			2.5	4	8	ms

All test items listed in Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C)

(1) Typ. value varies depending on the set value of detector threshold.

(2) Minimum value of power supply voltage when an output voltage becomes 0.1V or less at detection.
(Pulled-up resistance: 100 kΩ, Pulled-up voltage: 5 V)

V_{DD} = 14 V, C_D = 0.01 µF, pulled-up to 5 V with 100 kΩ, unless otherwise specfied.
The specifications surrounded by $\boxed{}$ are guaranteed by design engineering at -40°C ≤ Ta ≤ 125°C.

R3154N-YE Product-specific Electrical Characteristics

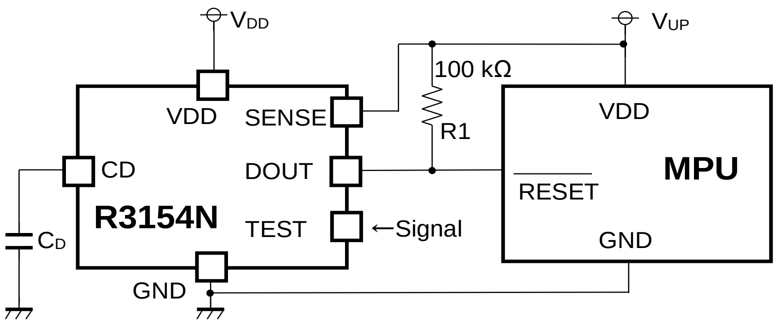
(Ta = 25°C)

Product name	V_{OVDET} (V)			V_{UVDET} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R3154N201A	0.85550	0.86	0.86450	0.76615	0.77	0.77385
R3154N202A	0.74550	0.75	0.75450	0.54670	0.55	0.55330
R3154N203A	3.52230	3.54	3.55770	3.03475	3.05	3.06525
R3154N204A	1.32335	1.33	1.33665	1.16415	1.17	1.17585
R3154N205A	1.07460	1.08	1.08540	0.91540	0.92	0.92460
R3154N206A	0.86550	0.87	0.87450	0.72635	0.73	0.73365

(-40°C ≤ Ta ≤ 125°C)

Product name	V_{OVDET} (V)			V_{UVDET} (V)			V_{OVHYS} (V)			V_{UVHYS} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
R3154N201A	$\boxed{0.84875}$	0.86	$\boxed{0.86675}$	$\boxed{0.76038}$	0.77	$\boxed{0.77577}$	$\boxed{0.00215}$	0.00430	$\boxed{0.00645}$	$\boxed{0.00193}$	0.00385	$\boxed{0.00577}$
R3154N202A	$\boxed{0.73875}$	0.75	$\boxed{0.75675}$	$\boxed{0.54175}$	0.55	$\boxed{0.55495}$	$\boxed{0.00188}$	0.00375	$\boxed{0.00562}$	$\boxed{0.00138}$	0.00275	$\boxed{0.00412}$
R3154N203A	$\boxed{3.49575}$	3.54	$\boxed{3.56655}$	$\boxed{3.01188}$	3.05	$\boxed{3.07287}$	$\boxed{0.00885}$	0.01770	$\boxed{0.02655}$	$\boxed{0.00763}$	0.01525	$\boxed{0.02287}$
R3154N204A	$\boxed{1.31338}$	1.33	$\boxed{1.33997}$	$\boxed{1.15538}$	1.17	$\boxed{1.17877}$	$\boxed{0.00333}$	0.00665	$\boxed{0.00997}$	$\boxed{0.00293}$	0.00585	$\boxed{0.00877}$
R3154N205A	$\boxed{1.06650}$	1.08	$\boxed{1.08810}$	$\boxed{0.90850}$	0.92	$\boxed{0.92690}$	$\boxed{0.00270}$	0.00540	$\boxed{0.00810}$	$\boxed{0.00230}$	0.00460	$\boxed{0.00690}$
R3154N206A	$\boxed{0.85875}$	0.87	$\boxed{0.87675}$	$\boxed{0.72088}$	0.73	$\boxed{0.73547}$	$\boxed{0.00218}$	0.00435	$\boxed{0.00652}$	$\boxed{0.00183}$	0.00365	$\boxed{0.00547}$

TYPICAL APPLICATION CIRCUIT

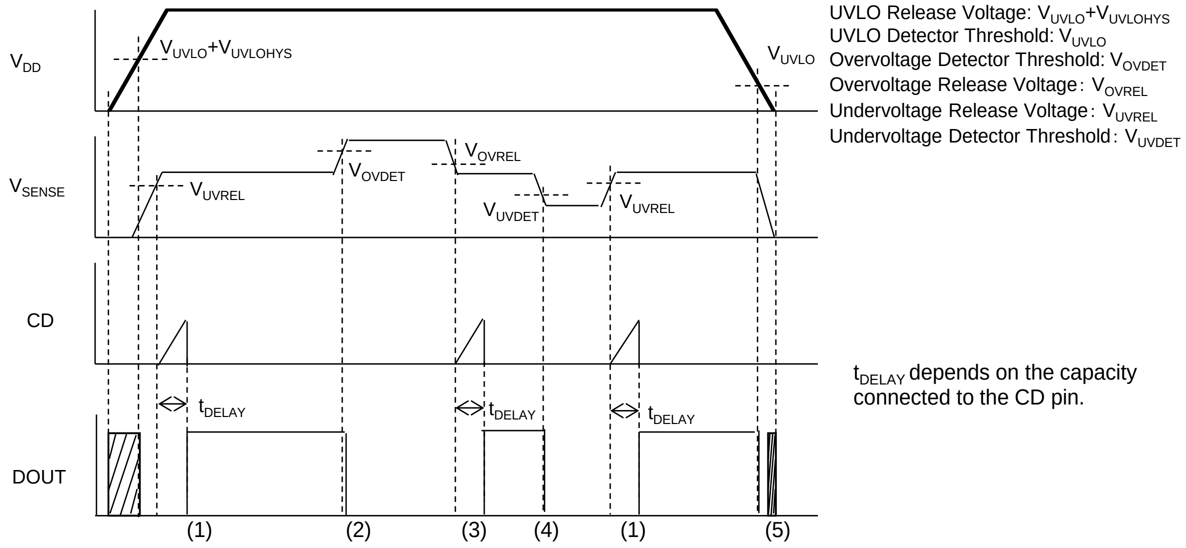


R3154N Typical Application Circuit

Recommended External Components

Symbol	Description
C_D	A capacitor should be selected corresponding to the set Release Delay Time. Refer to *"Delay in Operation and Release Delay Time (t_{DELAY})"* in THEORY OF OPERATION for details. When minimizing the release delay time, layout the circuit without any capacitor.
R1	The "Low" voltage of the DOUT output is determined by the division ratio of the on resistance of the NMOS driver and the pull-up resistance value (R1). The on-resistance of the NMOS driver is calculated from the "NMOS driver output current". Select the pull-up resistance value (R1) to bring the "Low" voltage of the DOUT output to the desired voltage. The "High" level of the DOUT output is determined by the division ratio of the leakage current of the NMOS driver and the pull-up resistance value (R1). The leakage current of the NMOS driver is calculated from the "NMOS driver leakage current". Confirm if the "High" voltage of the DOUT output is the desired voltage. *"Electrical Characteristic"* is evaluated in conditions that pull-up voltage = 5 V and R1 = 100 kΩ.

THEORY OF OPERATION



R3154N Timing Chart

(1) When the SENSE pin voltage (V_{SENSE}) exceeds the undervoltage release voltage (V_{UVREL}), the DOUT pin outputs "High" after the release delay time (t_{DELAY}).

(2) When V_{SENSE} exceeds the overvoltage detector threshold ($V_{OV\,DET}$) by increasing of the voltage, the DOUT pin outputs "Low" after the detection delay time (Typ. 20 μs) and this triggers the overvoltage detecting state.

(3) When V_{SENSE} decreases less than the overvoltage release voltage (V_{OVREL}), the DOUT pin outputs "High" after the release delay time (t_{DELAY}).

(4) When V_{SENSE} decreases less than the undervoltage detector threshold ($V_{UV\,DET}$), the DOUT pin outputs "Low" after the detection delay time (Typ. 20 μs) and this triggers the undervoltage detecting state.

(5) When the VDD pin voltage (V_{DD}) decreases less than the UVLO detector threshold (V_{UVLO}), the DOUT pin outputs "Low". Note that DOUT cannot maintain "Low" when the VDD pin voltage drops further and becomes lower than $V_{DDL.}$

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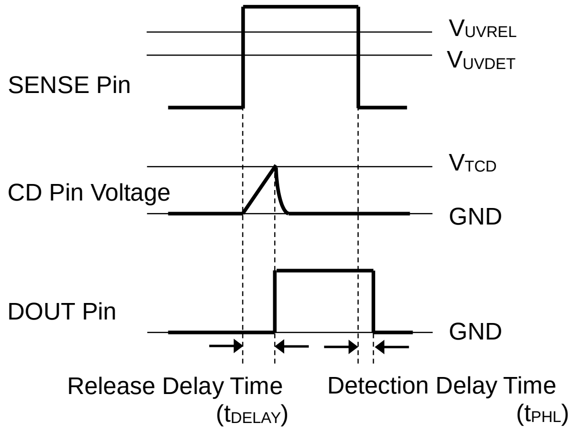
Delay Operation and Release Delay Time (t_{DELAY})

At Undervoltage Detection

A higher voltage than the undervoltage release voltage (V_{UVREL}) supplied to the SENSE pin triggers charging of the external capacitor (C_D capacitance), then the CD pin voltage (V_{CD}) increases. The DOUT pin voltage (V_{DOUT}) maintains "Low" until V_{CD} reaches the CD pin threshold voltage (V_{TCD}). When V_{CD} exceeds V_{TCD}, V_{DOUT} transitions from "Low" to "High". The release delay time (t_{DELAY}) is the period from the time the SENSE pin voltage (V_{SENSE}) exceeds V_{UVREL} to a rising edge of V_{DOUT}. V_{DOUT} transitions from "Low" to "High" and it leads to discharging of the C_D capacitor. Without the C_D capacitor, it becomes the short t_{DELAY} (Typ. 20 μs) depending on the circuit delay and CD pin stray capacity. When the higher voltage than V_{UVDET} is supplied to the SENSE pin, the detection delay time (t_{PHL}), which is the period that V_{DOUT} transitions from "High" to "Low", remains constant regardless of the capacitance value of the external capacitor.



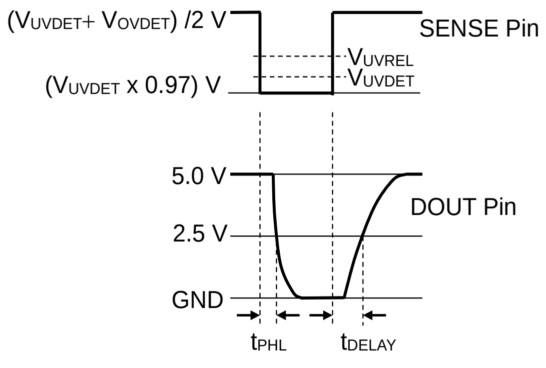
Undervoltage Release Delay Timing Chart

Calculation of Release Delay Time (t_{DELAY}) at Undervoltage Detection

The typical value of the release delay time (t_{DELAY}) with the capacitance of the external capacitor (C_D) is calculated in the following equation:

t_{DELAY} (s) = 0.73 × C_D (F) / (1.8×10^{-6})

t_{DELAYn} is the period until the DOUT pin voltage reaches 2.5 V after the pulse voltage of (V_{UVDET} + V_{OVDET}) /2 V increased from (V_{UVDET} x 0.97) V is supplied to the SENSE pin when DOUT pin is pulled up to 5 V with 100 kΩ.



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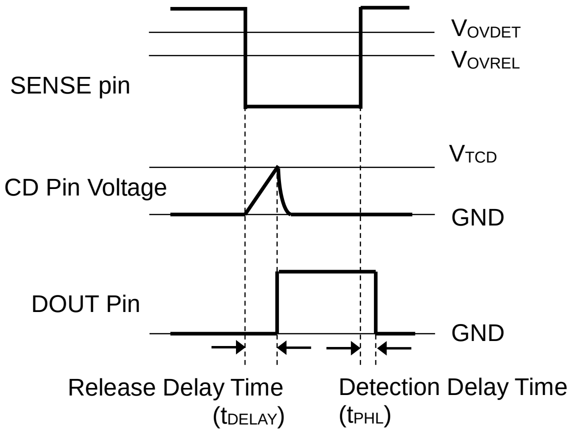
At Overvoltage Detection

A lower voltage than the overvoltage release voltage (V_{OVREL}) supplied to the SENSE pin triggers charging of the external capacitor (C_D capacitance), then the CD pin voltage (V_{CD}) increases. The DOUT pin voltage (V_{DOUT}) maintains “Low” until V_{CD} reaches the CD pin threshold voltage (V_{TCD}). When V_{CD} exceeds V_{TCD}, V_{DOUT} is inverted from “Low” to “High”. The release delay time (t_{DELAY}) is the period from the time the SENSE pin voltage (V_{SENSE}) falls below V_{OVREL} to a rising edge of V_{DOUT}. V_{DOUT} transitions to “High”. V_{DOUT} transitions from “Low” to “High” and it leads to discharging of the C_D capacitor. Without the C_D capacitor, it becomes the short t_{DELAY} (Typ. 20 μs) depending on the circuit delay and CD pin stray capacity. When the higher voltage than V_{OVDET} is supplied to the SENSE pin, the detection delay time (t_{PHL}), which is the period that V_{DOUT} transitions from “High” to “Low”, remains constant regardless of the capacitance value of the external capacitor.



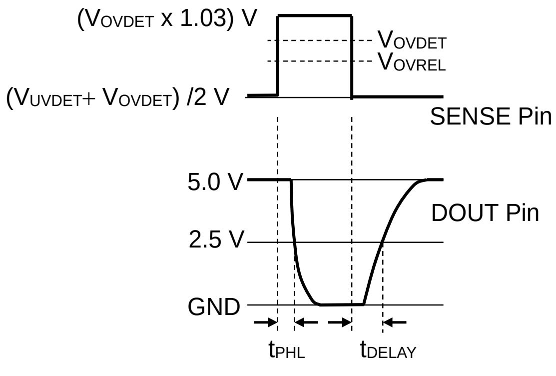
Overvoltage Release Delay Timing Chart

Calculation of Release Delay Time (t_{DELAY}) at Overvoltage Detection

The typical value of the release delay time (t_{DELAY}) with the capacitance of the external capacitor (C_D) is calculated in the following equation:

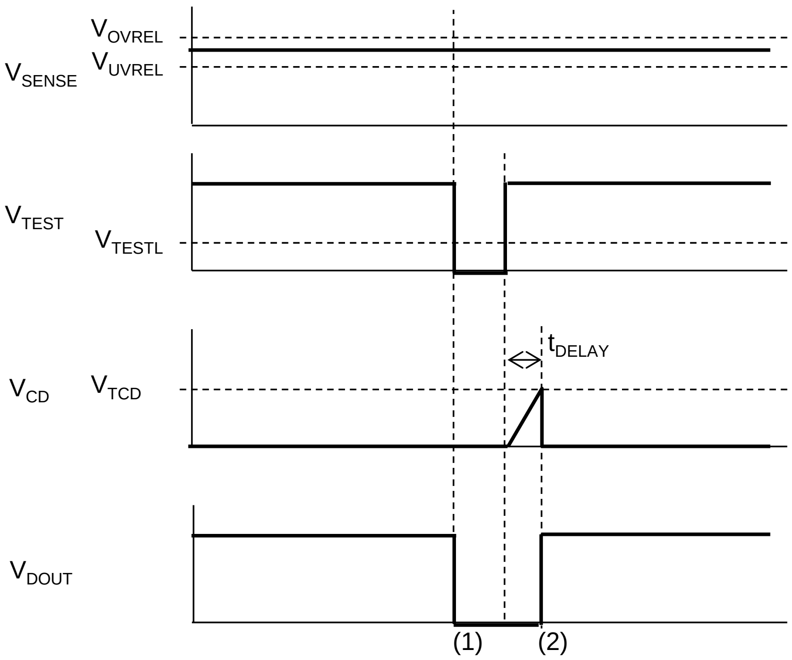
t_{DELAY} (s) = $0.73 \times C_D$ (F) / (1.8×10^{-6})

t_{DELAY} is the period until the DOUT pin voltage reaches 2.5 V after the pulse voltage of (V_{UVDET} + V_{OVDET}) /2 V decreased from (V_{OVDET} x 1.03) V is supplied to the SENSE pin when DOUT pin is pulled up to 5 V with 100 kΩ.



Operation Check of Voltage Detection Function with TEST Pin

Voltage Detection Function is to set DOUT to “Low” by inputting "Low" to the TEST pin, even when the SENSE pin voltage (V_{SENSE}) is within a range of the release voltage. If the DOUT does not become "Low" even V_{SENSE} is within the release voltage range and “Low” signal is input to the TEST pin, it can be judged that the IC has a fault. To cancel this function, set the TEST pin to "High" voltage or “Open”. When the TEST pin is open, the DOUT becomes "High" with pulled-up voltage in the IC.



TEST Pin Timing Chart

(1) When inputting “Low” to the TEST pin, the DOUT is fixed to "Low" after the detection delay time (Typ. 20 µs) even if the SENSE pin voltage (V_{SENSE}) is within a range of the release voltage. The “Low” signal of TEST pin voltage should be 50 µs or more.

(2) When the TEST pin transitions from "Low" to "High", the DOUT pin outputs "High" after the release delay time (t_{DELAY}). At this time, the TEST pin should maintain "High" for the release delay time or longer. Even when the external capacitor (C_D capacitance) is not connected, it should maintain "High" for 50 µs or more.

■ APPLICATION INFORMATION

The concept of “H” level of TEST pin

The R3154 has a voltage regulator (INT regulator) inside the IC. Major functions of the IC are operated by VCC (Typ. 3.3V) generated by INT regulator from input voltage, VDD.

TEST pin is pulled up to VCC voltage via 100kΩ as it can be set to open when TEST pin is unused.

When the voltage detect function is in use, when input “Low” voltage to TEST pin, then DOUT pin becomes “Low”. But when the voltage detect function is in no use, if “High” voltage is input to TEST pin, the current which is determined by the following equation flows continuously. This makes the supply current increase.

(VCC – TEST ”High” voltage) /100kΩ (VCC＞TEST ”High” voltage)

Unless there’s a specific reason to avoid an OPEN pin condition, it’s recommended to be left OPEN when TEST pin is not used.

As the circuit configuration prevents a reverse current from TEST pin to VCC, even when being used in condition of TEST “High” voltage＞VCC, supply current doesn’t increase and VCC voltage doesn’t vary.

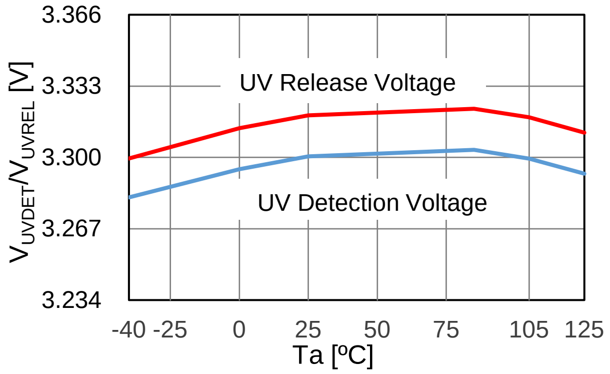
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

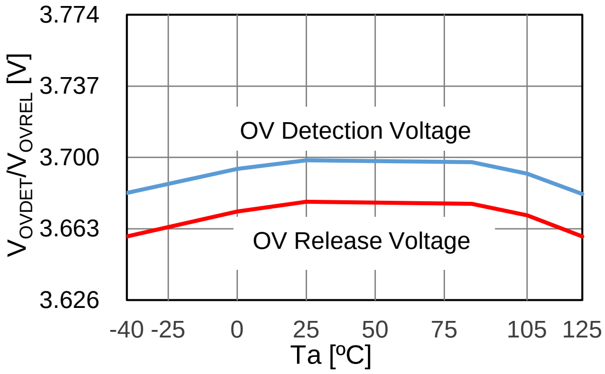
1) UV/OV Detection Release Voltage vs. Temperature

V_{DD} = 14 V,

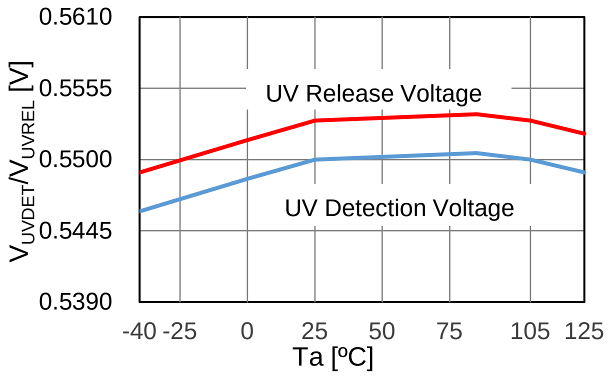
V_{UVSET} = 3.3V



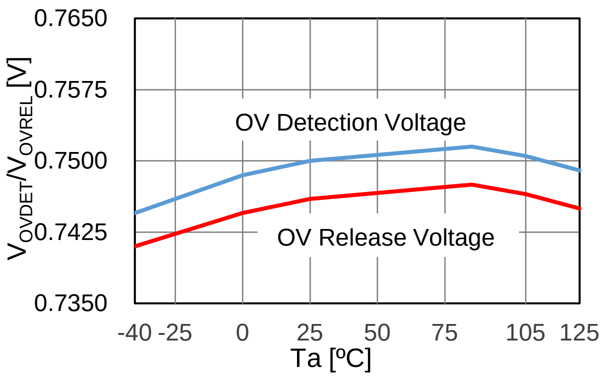
V_{OVSET} = 3.7 V



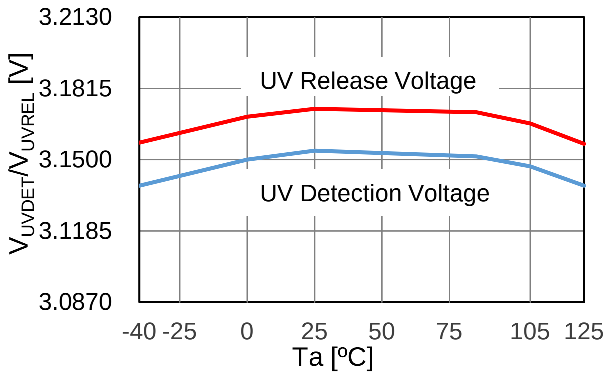
V_{UVSET} = 0.55V



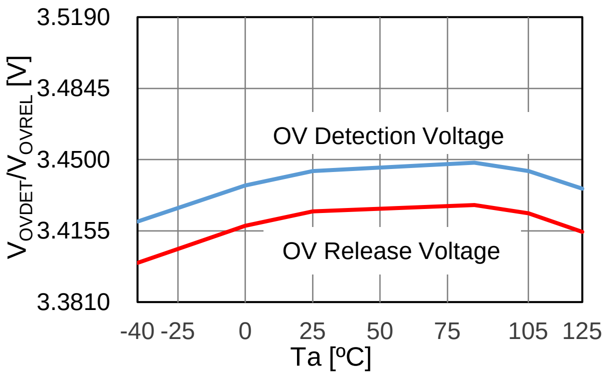
V_{OVSET} = 0.75 V



V_{UVSET} = 3.15V



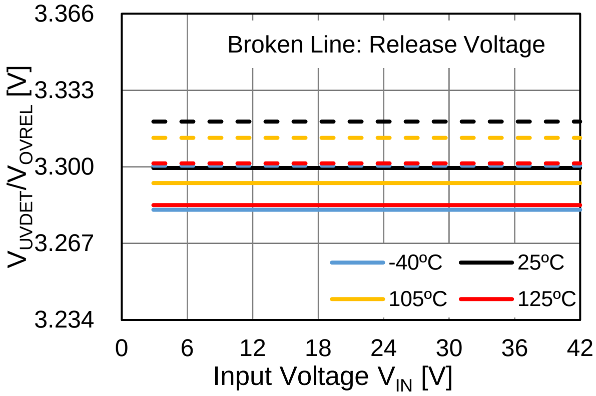
V_{OVSET} = 3.45 V



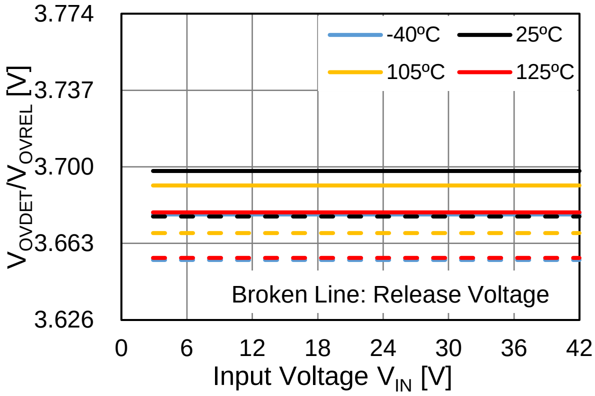
2) UV/OV Detection Voltage vs. Input Voltage

V_{DD} = 14 V,

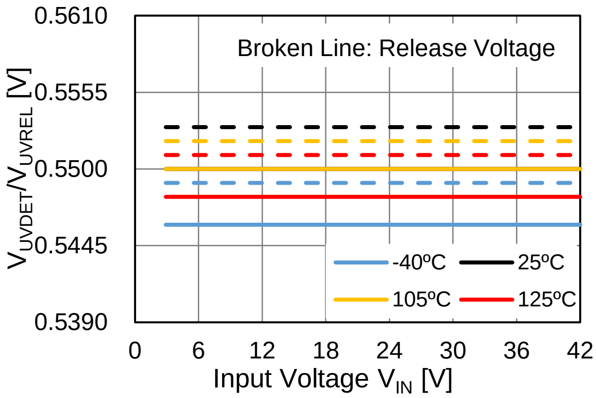
V_{UVSET} = 3.3V



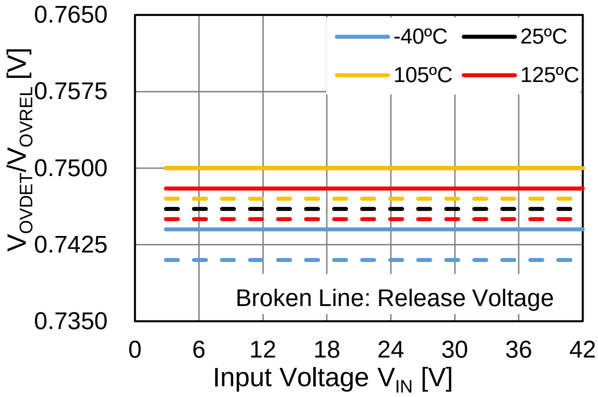
V_{OVSET} = 3.7 V



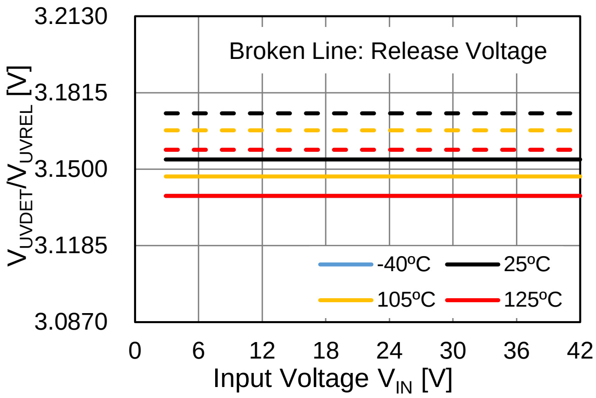
V_{UVSET} = 0.55V



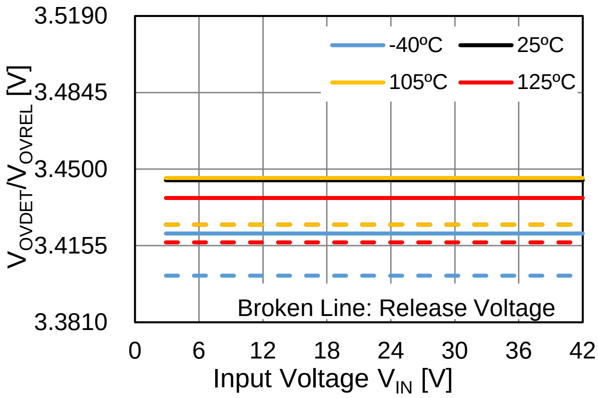
V_{OVSET} = 0.75 V



V_{UVSET} = 3.15V

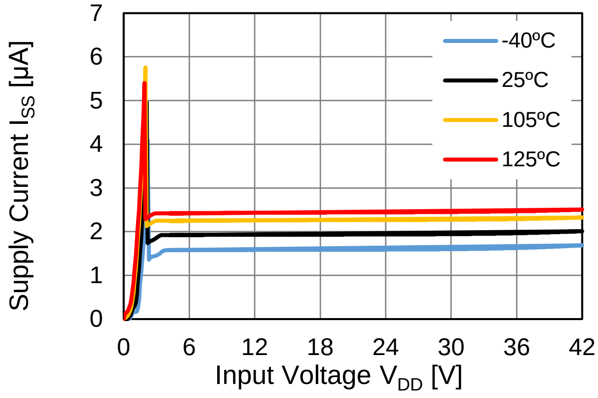


V_{OVSET} = 3.45 V



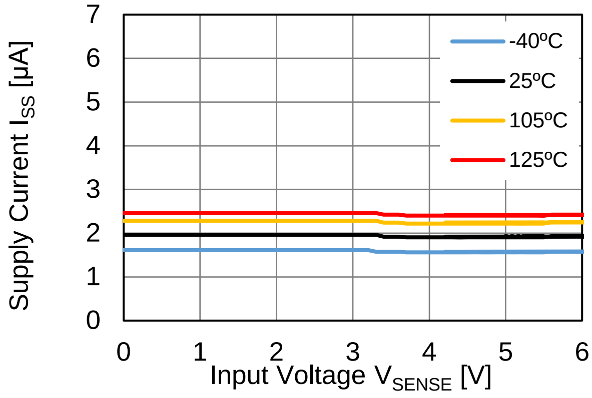
3) Supply Current vs. Input Voltage

V_{UVSET} = 3.3 V / V_{OVSET} = 3.7 V, V_{SENSE} = 3.5V



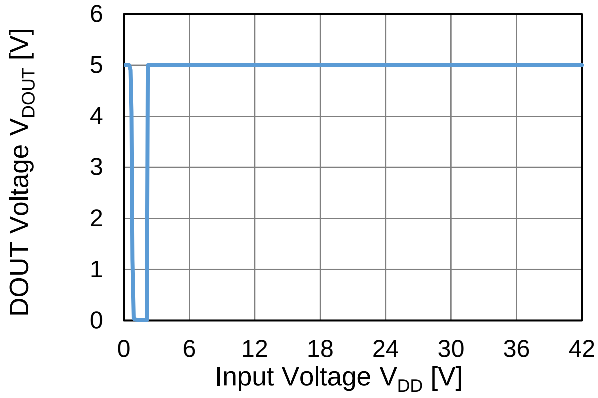
4) Supply Current vs. V_{SENSE}

V_{UVSET} = 3.3 V / V_{OVSET} = 3.7 V, V_{DD} = 14 V



5) DOUT Pin Voltage vs. Input Voltage

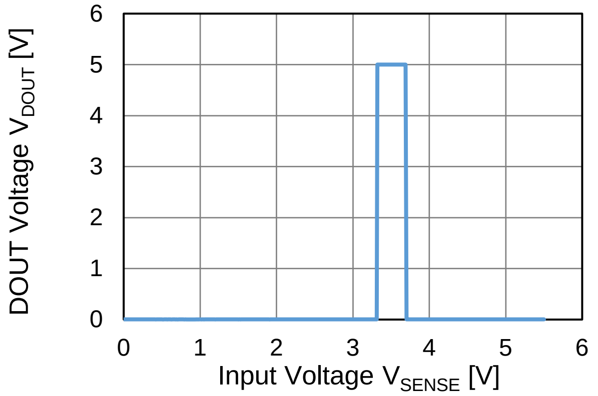
V_{UVSET} = 3.3 V/V_{OVSET} = 3.7 V, V_{SENSE} = 3.5V, Ta = 25ºC



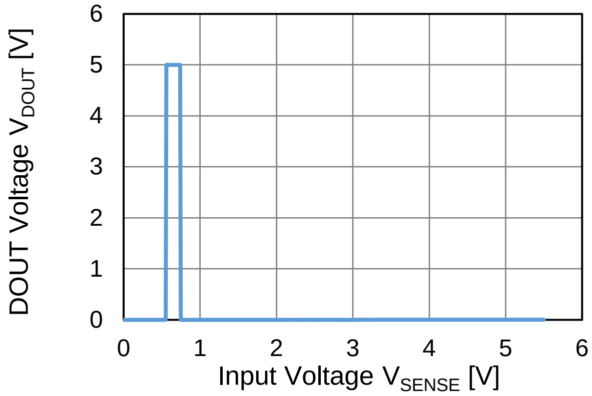
6) DOUT Pin Voltage vs. V_{SENSE}

V_{DD} = 14 V, Ta = 25ºC,

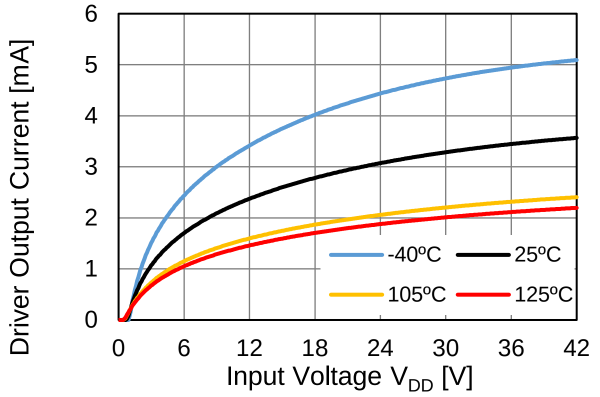
V_{UVSET} = 3.3 V / V_{OVSET} = 3.7 V



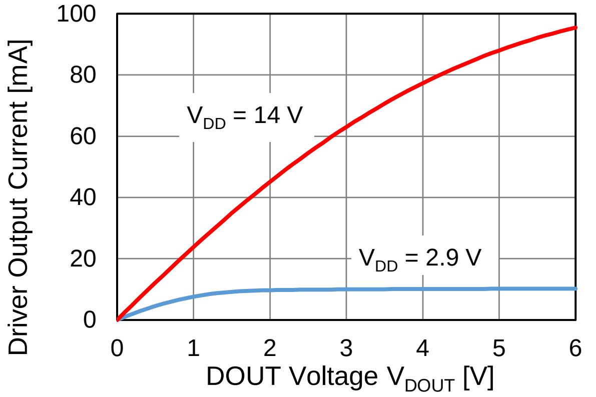
V_{UVSET} = 0.55 V / V_{OVSET} = 0.75 V



7) Driver Output Current vs. Input Voltage
V_{SENSE} = 0 V, D_{OUT} = 0.1 V

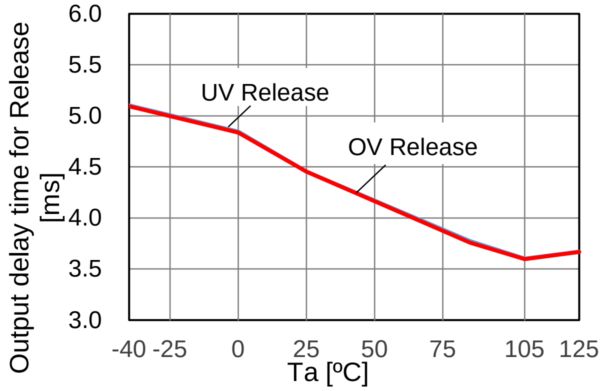


8) Driver Output Current vs. DOUT Pin Voltage
V_{SENSE} = 0 V, Ta = 25ºC



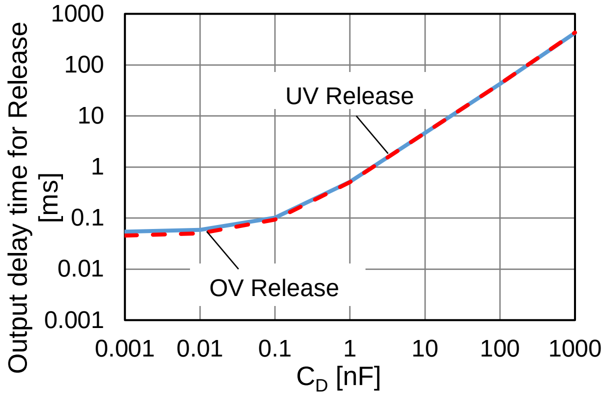
9) Release Delay Time vs. Temperature

V_{UVSET} = 3.3 V/V_{OVSET} = 3.7 V, V_{DD} = 14 V, C_D = 10 nF

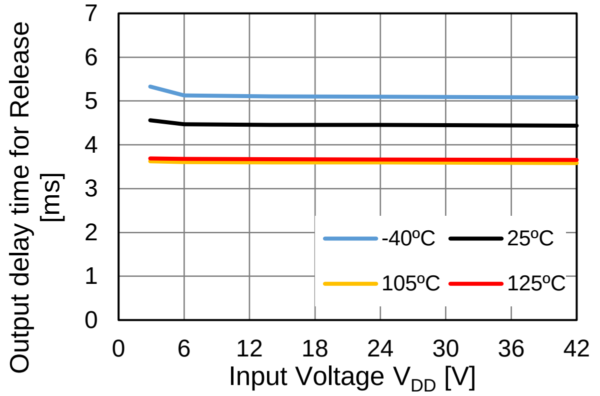


10) Release Delay Time vs. External Capacitor for CD Pin

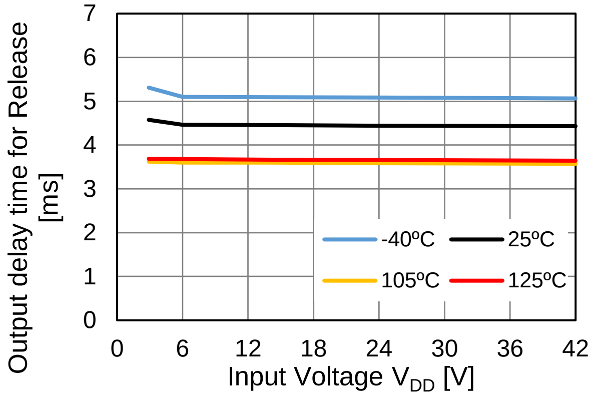
V_{UVSET} = 3.3 V/V_{OVSET} = 3.7 V, V_{DD} = 14 V, Ta = 25ºC



11) Release Delay Time vs. Input Voltage
C_D = 10 nF
V_{SENSE} = 0 V → (V_{UVSET} + V_{OVSET}) / 2



V_{SENSE} = 5.5 V → (V_{UVSET} + V_{OVSET}) / 2



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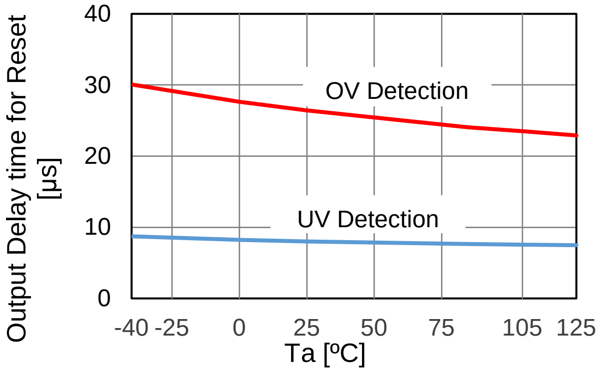
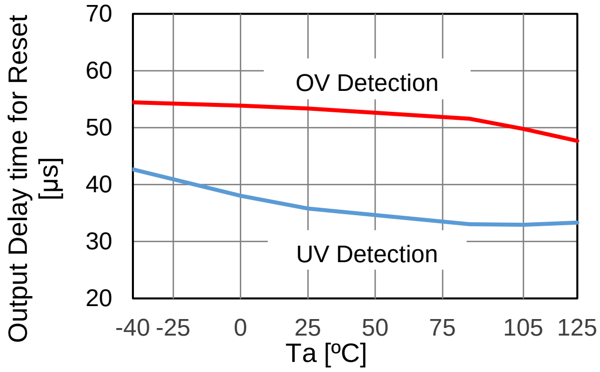
12) Detection Delay Time vs. Temperature

V_{DD} = 14 V, V_{UVSET} = 3.3 V / V_{OVSET} = 3.7 V

V_{SENSE} = 3.5 V → 0 V (UV), 3.5 V → 5.5 V (OV)

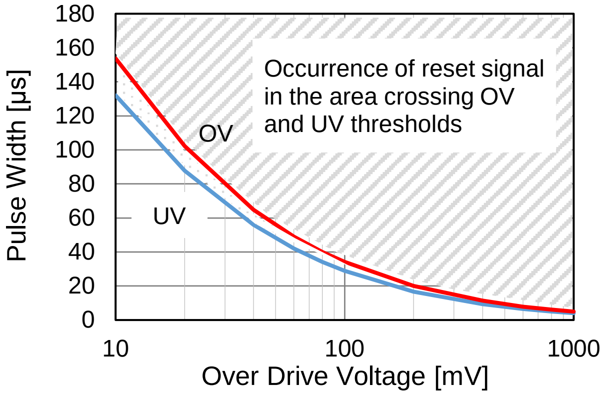


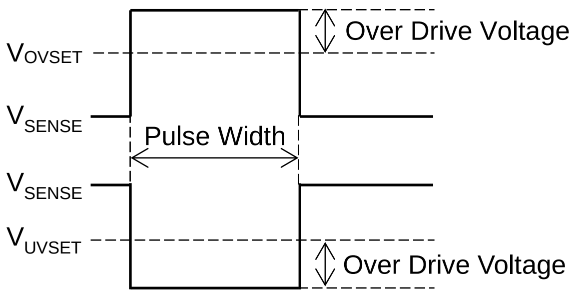
V_{SENSE} = 3.5 V → 3.2 V (UV), 3.5 V → 3.81 V (OV)



13) SENSE Pulse Width vs. Over Drive Voltage

V_{DD} = 14 V, V_{UVSET} = 3.3 V / V_{OVSET} = 3.7 V, Ta = 25ºC





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PD-SOT-23-6-(125150)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

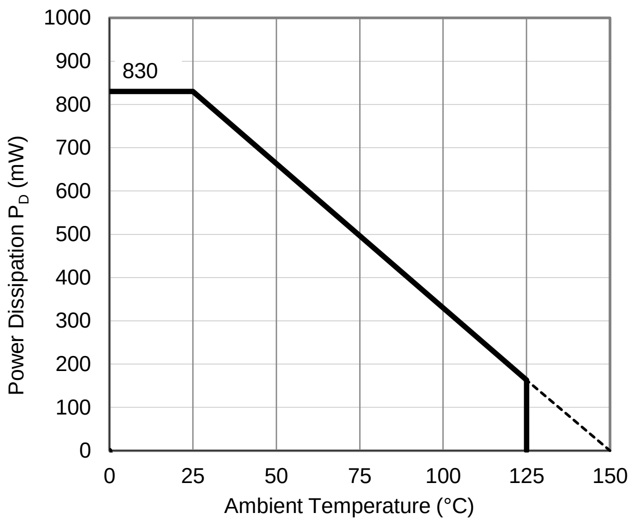
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 7 pcs

Measurement Result (Ta = 25°C, Tjmax = 150°C)

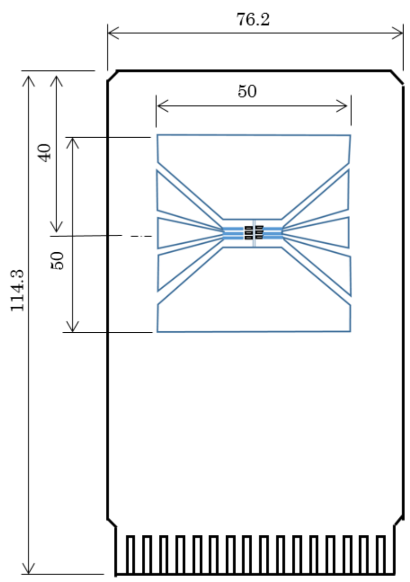
Item	Measurement Result
Power Dissipation	830 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

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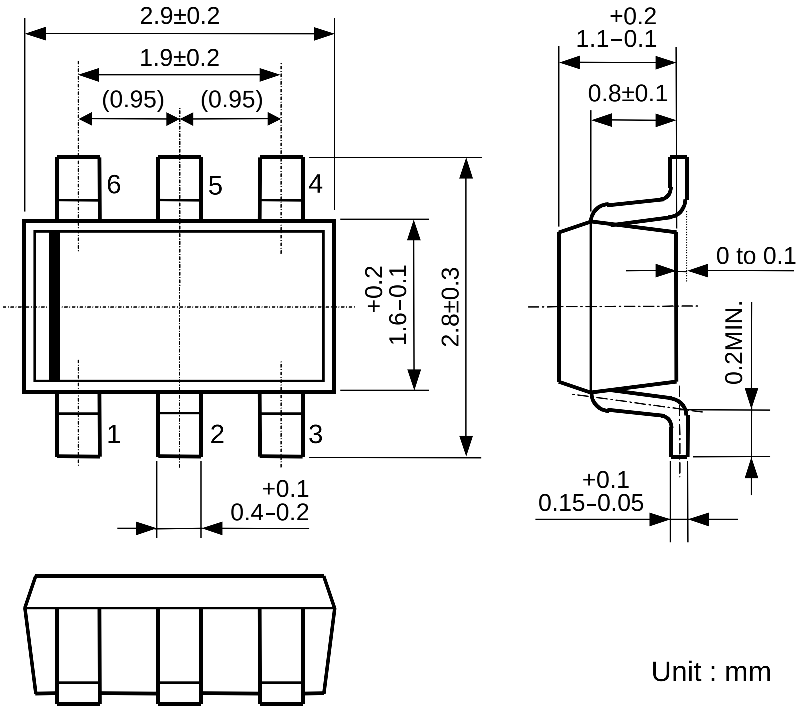
DM-SOT-23-6-JE-B



SOT-23-6 Package Dimensions (Unit: mm)

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