RICOH

R5439K Series

2 to 4 Serial Cell Li-Ion or Li-Polymer Battery Protection IC for Secondary Protection

NO.EA-349-201105

OUTLINE

The R5439K is an overcharge protection IC for 2 to 4 serial cell Li-ion or Li-polymer secondary battery. Internally, the R5439K consists of high-accuracy voltage detection circuit, a delay circuit, and a voltage regulator for operating the external real-time clock. The two-stage shut-down detection circuit can reduce the supply current to the minimum.

FEATURES

- High Voltage Tolerant Process
  Absolute Maximum Ratings ..... 32 V
- Low Supply Current
  During Operation, Cell-voltage: 4.15 V, 4-Cells..... Typ. 4.0 µA
  Shutdown 1 ..... Typ. 2.5 µA
  Shutdown 2 (Standby) ..... Max. 0.2 µA
- Output Voltage
  Built-in Regulator..... 2.9 V to 3.7 V, 0.1 V step
  Output Voltage Accuracy..... ±2%
  COUT Output (CMOS Output, Active-high)..... Typ. 4.7 V
- High-accuracy Voltage Detection
  Overcharge Detector Threshold (V_{DET1n}[(1)])..... 4.20 V to 4.65 V, in 5 mV step
  Overcharge Detector Threshold Accuracy ..... ± 0.02 V (Ta = 25°C)
  ± 0.025 V (0°C < Ta < 60°C)
  Overcharge Release Voltage (V_{REL1n}[(1)])..... V_{DET1n}−0V to V_{DET1n}−0.4V, in 50 mV step
  Min.4.15V
  Overcharge Detection Delay Time ..... 2-, 4-, or 6-sec with Delay Time Shortening Function[(2)]
  Overcharge Release Voltage Condition ..... Voltage Release Type
- Shutdown Functions
  [Shutdown 1]
  Shutdown 1 Detector Threshold..... Typ. 3.8 V, ±0.3 V
  Shutdown 1 Detection Delay Time..... none
  [Shutdown 2]
  Shutdown 2 Detector Threshold (V_{SHT2n}[(1)])..... 2.3 V to 2.8 V, 100 mV step
  Shutdown 2 Detector Threshold Accuracy..... ±0.05 V
  Shutdown 2 Release Voltage ..... V_{SHT2n} + 0.2 V
  Shutdown 2 Detection Delay Time..... 2-, 4-, or 6-sec
- 2 to 4 Cells Selectable Battery Protection
- Timer Reset Delay Function
- Compact Package
  DFN (PLP) 2020-8..... 2.0 mm x 2.0 mm

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(1) V_{DET1n}, V_{REL1n}, V_{SHT2n} : n =1, 2, 3, 4

(2) The delay time can be reduced down to approx. 1/80 by applying a 4 V ± 0.2 V to the VDD – VC1 pins.

APPLICATIONS

- Li-Ion or Li-Polymer Battery Protection

SELECTION GUIDE

The overcharge and the delay time are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5439Kxxx$∗-TR	DFN (PLP) 2020-8	5,000 pcs	Yes	Yes

xxx: Specify the combination of the overcharge detector threshold (V_{DET1n}), the overcharge release voltage (V_{REL1n}), the shutdown 2 detector threshold (V_{SHT2n}) and the voltage regulator output voltage (V_{ROUT}) [(1)].

V_{DET1n}[(2)]: 4.20 V to 4.65 V in 5 mV step
V_{REL1n}[(2)]: V_{DET1n} – 0 V to V_{DET1n} – 0.4 V in 50 mV step, Min. 4.15 V
V_{SHT2n}[(2)]: 2.3 V to 2.8 V in 100 mV step
V_{ROUT}: 2.9 V to 3.7 V in 0.1 V step

$: Specify the combination of the overcharge detection delay time (t_{VDET1}), the shutdown 2 detection delay time (t_{VSHT2}) and the overcharge release delay time (t_{VREL1}) and the overcharge detection timer reset delay time (t_{VTR}). Refer to *Delay Time Code Table* for details.

Delay Time Code Table

Code	t_{VDET1} (s)	t_{VSHT2} (s)	t_{VREL1} (ms)	t_{VTR} (ms)
A	2	2	16	6
B	4	2	16	6
C	6	2	16	6
D	2	4	16	6
E	4	4	16	6
F	6	4	16	6
G	2	6	16	6
H	4	6	16	6
J	6	6	16	6
K	1.5	4.5	12	4.5

∗: Specify the timer reset delay time option. Refer to *Timer Reset Delay Time Table* for details.

Timer Reset Delay Time Table

Code	Timer Reset Delay Time
A	No
B	Yes

(1) Refer to *Product Code Table* for details.
(2) V_{DET1n}, V_{REL1n}, V_{SHT2n}: n = 1, 2, 3, 4

● Product Code List

The product code is determined by the combination of the set output voltage (overcharge detector threshold: V_{DET1n}, overcharge release voltage: V_{REL1n}, shutdown 2 detector threshold: V_{SHT2n}, voltage regulator output voltage: V_{ROUT}) and the delay time (overcharge detection delay time: t_{VDET1}, shutdown 2 detection delay time: t_{VSHT2}, overcharge release delay time: t_{VREL1}, overcharge detection timer reset delay time: t_{VTR}) and the timer reset delay time option (t_{VTR}).

Product Code Table

Product Name	Set Output Voltage (V)				Delay Time				Timer Reset Delay Time (Yes/No[1])
	V_{DET1n}	V_{REL1n}	V_{SHT2n}	V_{ROUT}	t_{VDET1} (s)	t_{VSHT2} (s)	t_{VREL1} (ms)	t_{VTR} (ms)	
R5439K213HA	4.450	4.250	2.500	2.900	4	6	16	—	No
R5439K301GA	4.450	4.150	2.500	3.300	2	6	16	—	No
R5439K301HA	4.450	4.150	2.500	3.300	4	6	16	—	No
R5439K309GA	4.300	4.150	2.500	3.300	2	6	16	—	No
R5439K309HA	4.300	4.150	2.500	3.300	4	6	16	—	No
R5439K310GA	4.350	4.150	2.500	3.300	2	6	16	—	No
R5439K310HA	4.350	4.150	2.500	3.300	4	6	16	—	No
R5439K310KA	4.350	4.150	2.500	3.300	1.5	4.5	12	—	No
R5439K310JB	4.350	4.150	2.500	3.300	6	6	16	6	Yes
R5439K311GA	4.400	4.150	2.500	3.300	2	6	16	—	No
R5439K311HA	4.400	4.150	2.500	3.300	4	6	16	—	No
R5439K312GA	4.550	4.150	2.500	3.300	2	6	16	—	No
R5439K312HA	4.550	4.150	2.500	3.300	4	6	16	—	No
R5439K313JB	4.450	4.250	2.500	3.300	6	6	16	6	Yes
R5439K313KA	4.450	4.250	2.500	3.300	1.5	4.5	12	—	No
R5439K314JB	4.500	4.300	2.500	3.300	6	6	16	6	Yes
R5439K314HA	4.500	4.300	2.500	3.300	4	6	16	—	No
R5439K314KA	4.500	4.300	2.500	3.300	1.5	4.5	12	—	No
R5439K316JB	4.400	4.200	2.500	3.300	6	6	16	6	Yes
R5439K316KA	4.400	4.200	2.500	3.300	1.5	4.5	12	—	No
R5439K317JB	4.500	4.200	2.500	3.300	6	6	16	6	Yes
R5439K318KA	4.325	4.150	2.500	3.300	1.5	4.5	12	—	No
R5439K319JB	4.550	4.350	2.500	3.300	6	6	16	6	Yes
R5439K320KA	4.500	4.300	2.500	3.100	1.5	4.5	12	—	No
R5439K321KA	4.500	4.300	2.500	3.200	1.5	4.5	12	—	No
R5439K323JB	4.550	4.250	2.500	3.000	6	6	16	6	Yes
R5439K324JB	4.500	4.200	2.500	3.000	6	6	16	6	Yes
R5439K325JB	4.500	4.300	2.800	3.300	6	6	16	6	Yes
R5439K326JB	4.220	4.150	2.500	3.300	6	6	16	6	Yes
R5439K327JB	4.600	4.300	2.500	3.000	6	6	16	6	Yes
R5439K328JB	4.600	4.300	2.500	3.300	6	6	16	6	Yes

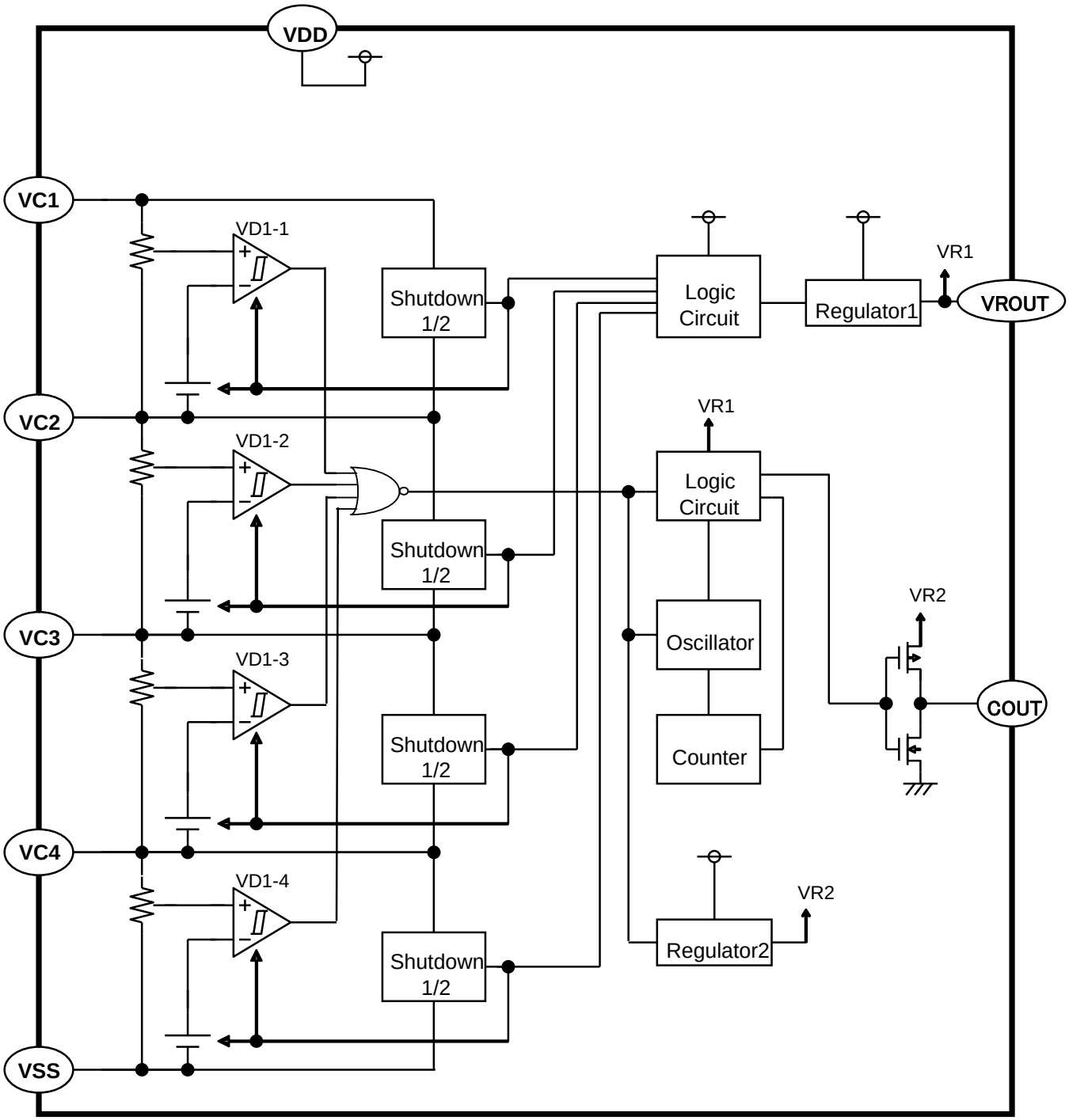
(1) "No" means the timer reset delay time option is absence.

Product Code Table (Continued)

Product Name	Set Output Voltage (V)				Delay Time				Timer Reset Delay Time (Yes/No[1])
	V_{DET1n}	V_{REL1n}	V_{SHT2n}	V_{ROUT}	t_{VDET1} (s)	t_{VSHT2} (s)	t_{VREL1} (ms)	t_{VTR} (ms)	
R5439K314JA	4.500	4.300	2.500	3.300	6	6	16	—	No
R5439K317JA	4.500	4.200	2.500	3.300	6	6	16	—	No
R5439K319JA	4.550	4.350	2.500	3.300	6	6	16	—	No
R5439K323JA	4.550	4.250	2.500	3.000	6	6	16	—	No
R5439K327JA	4.600	4.300	2.500	3.000	6	6	16	—	No
R5439K328JA	4.600	4.300	2.500	3.300	6	6	16	—	No
R5439K329JA	4.550	4.250	2.500	3.300	6	6	16	—	No
R5439K330JA	4.550	4.250	2.800	3.300	6	6	16	—	No
R5439K331JA	4.600	4.300	2.800	3.300	6	6	16	—	No
R5439K332JA	4.450	4.150	2.800	3.300	6	6	16	—	No
R5439K333JA	4.450	4.150	2.500	3.000	6	6	16	—	No
R5439K334JA	4.650	4.350	2.500	3.300	6	6	16	—	No

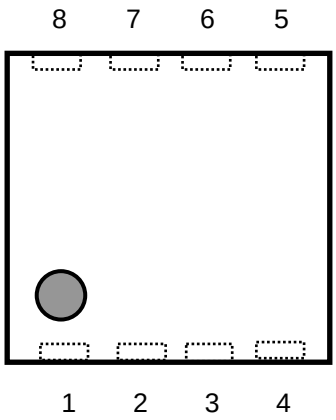
(1) "No" means the timer reset delay time option is absence.

BLOCK DIAGRAM



PIN DESCRIPTIONS

DFN(PLP)2020-8



DFN(PLP)2020-8 Pin Description

Pin No.	Symbol	Description
1	VDD	Power Supply Pin
2	VC1	CELL1 Plus Pin
3	VC2	CELL2 Plus Pin
4	VC3	CELL3 Plus Pin
5	VC4	CELL4 Plus Pin
6	VSS	IC Ground Pin
7	COUT	Overcharge Detection Output Pin
8	VROUT	Voltage Regulator Output Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0 V)

Symbol	Item	Rating	Unit
V_{DD}	Power Supply Voltage	V_{C1} − 0.3 to V_{C1} + 6.5 V_{C1} − 0.3 to 32	V
V_{C1}	CELL1 Plus Pin Input Voltage	V_{C2} − 0.3 to V_{C2} + 6.5	V
V_{C2}	CELL2 Plus Pin Input Voltage	V_{C3} − 0.3 to V_{C3} + 6.5	V
V_{C3}	CELL3 Plus Pin Input Voltage	V_{C4} − 0.3 to V_{C4} + 6.5	V
V_{C4}	CELL4 Plus Pin Input Voltage	−0.3 to 6.5	V
V_{COUT}	COUT Pin Output Voltage	−0.3 to V_{OH1} + 0.3	V
V_{ROUT}	VR Output Voltage	−0.3 to 6.5	V
I_{OUT}	VR Output Current	3	mA
P_D	Power Dissipation	Refer to Appendix “Power Dissipation”.	
Tj	Junction Temperature Range	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITION

Symbol	Item	Rating	Unit
V_{DD}	Operating Input Voltage	4.0 to 25 / V_{C1} +5.0	V
V_{C1}	CELL1 Plus Pin Input Voltage	V_{C2} + 1.2 to V_{C2} + 5.0	V
	(in 2-/3-cell mode)	V_{C2} + 0.0	
V_{C2}	CELL2 Plus Pin Input Voltage	V_{C3} + 1.2 to V_{C3} + 5.0	V
	(in 2-cell mode)	V_{C3} + 0.0	
V_{C3}	CELL3 Plus Pin Input Voltage	V_{C4} + 1.2 to V_{C4} + 5.0	V
V_{C4}	CELL4 Plus Pin Input Voltage	V_{SS} + 1.2 to V_{SS} + 5.0	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{CELLn} = CELLn (Ex. V_{CELL1} is a voltage difference between VC1 and VC2)

n = 1, 2, 3, 4, unless otherwise noted

The specifications surrounded by ☐ are guaranteed by Design Engineering at 0°C ≤ Ta ≤ 60°C.

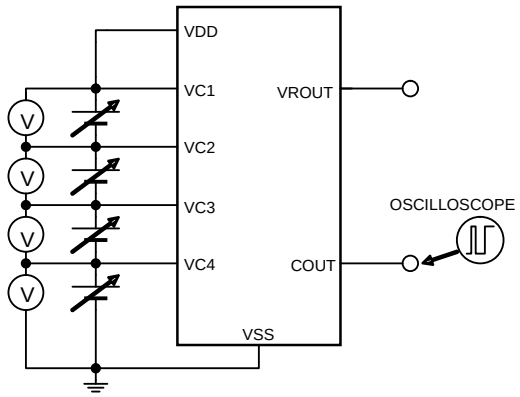
R5439K Electrical Characteristics (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	Circuit (1)
V_{DET1n}	CELLn Overcharge Detection Threshold	It detects rising edge of supply voltage.	V_{DET1n} −0.020V ☐ V_{DET1n} −0.025V ☐	V_{DET1n}	V_{DET1n} +0.020V ☐ V_{DET1n} +0.025V ☐	V	A
V_{REL1n}	CELLn Overcharge Release Voltage	It detects falling edge of supply voltage.	V_{REL1n} −0.050V	V_{REL1n}	V_{REL1n} +0.050V	V	A
t_{VDET1}	Overcharge Detection Delay Time	V_{CELLn} = 4.15 V (n = 2, 3, 4) V_{CELL1} = 4.15 V → 4.7 V	t_{VDET1} x 0.8	t_{VDET1}	t_{VDET1} x 1.2	s	B
t_{VREL1}	Overcharge Release Delay Time	V_{CELLn} = 3.9 V (n = 2, 3, 4) V_{CELL1} = 4.7 V → 3.9 V	t_{VREL1} x 0.8	t_{VREL1}	t_{VREL1} x 1.2	ms	B
t_{VTR}	Overcharge Detection Timer Reset Delay Time (For the Timer Reset Delay function type only)	V_{CELLn} = V_{DET1n} + 0.05 V → V_{REL1n} −0.10 V → V_{DET1n} +0.05 V → V_{REL1n} −0.10 V	2 1.5(2)	6 4.5(2)	10 7.5(2)	ms	B
V_{SHT1n}	Shutdown 1 Detector Threshold	It detects falling edge of supply voltage.	3.5	3.8	4.1	V	C
V_{SHT2n}	Shutdown 2 Detector Threshold	It detects falling edge of supply voltage.	V_{SHT2n} −0.050V	V_{SHT2n}	V_{SHT2n} +0.050V	V	I
V_{REL2n}	Shutdown 2 Release Voltage	It detects rising edge of supply voltage.	V_{REL2n} −0.100V	V_{REL2n} (V_{SHT2n} +0.2V)	V_{REL2n} +0.100V	V	I
t_{VSHT2}	Shutdown 2 Detector Delay Time	V_{CELLn} = V_{SHT2n} −0.2 V (n = 2, 3, 4) V_{CELL1} = 3.2 V → V_{SHT2n} −0.2 V	t_{VSHT2} x 0.8	t_{VSHT2}	t_{VSHT2} x 1.2	s	J
V_{OL}	C_{OUT} Nch ON Voltage	I_{OL} = 50 μA, V_{CELLn} = 4.15 V (n = 1, 2, 3, 4)		0.1	0.5	V	F
V_{OH1}	C_{OUT} Pch ON Voltage 1	I_{OH} = 0 μA, V_{CELLn} = 4.7 V	4.0	4.7	5.4	V	D
V_{OH2}	C_{OUT} Pch ON Voltage 2	I_{OH} = −50 μA, V_{CELLn} = 4.7 V	V_{OH1} −0.5V	V_{OH1} −0.1V		V	E
I_{SHT1}	Shutdown 1 Current	V_{CELLn} = 3.1 V		2.5	5.75	μA	G
I_{SHT2}	Shutdown 2 Current	V_{CELLn} = 2.0 V			0.2	μA	G
I_{SS}	Supply Current	V_{CELLn} = 4.15 V		4.0	7.5	μA	G
I_{VDD}	VDD Pin Current	V_{CELLn} = 4.15 V		2.4	5.2	μA	K
I_{VC1}	VC1 Pin Current	V_{CELLn} = 4.15 V		1.6	2.8	μA	K
I_{VC2}	VC2 Pin Current	V_{CELLn} = 4.15 V	−0.3		0.3	μA	K
I_{VC3}	VC3 Pin Current	V_{CELLn} = 4.15 V	−0.3		0.3	μA	K
I_{VC4}	VC4 Pin Current	V_{CELLn} = 4.15 V	−0.3		0.3	μA	K
V_{ROUT}	VR Output Voltage	V_{SHT2n}x2+0.1V ≤ V_{DD} ≤ 25V, I_{OUT} =10μA	V_{ROUT} x 0.98	V_{ROUT}	V_{ROUT} x 1.02	V	H
I_{OUT}	VR Output Current	V_{SHT2n}x2+0.1V ≤ V_{DD} ≤ 25V			2	mA	H

(1) Refer to *TEST CIRCUITS* for detail information.
(2) The delay time code is K only.

TEST CIRCUITS

A



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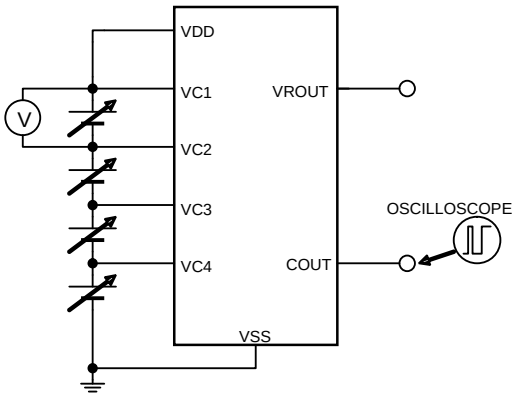

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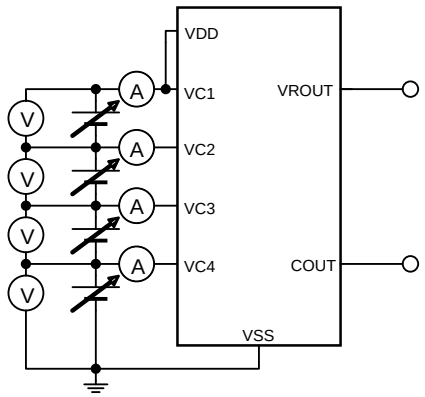

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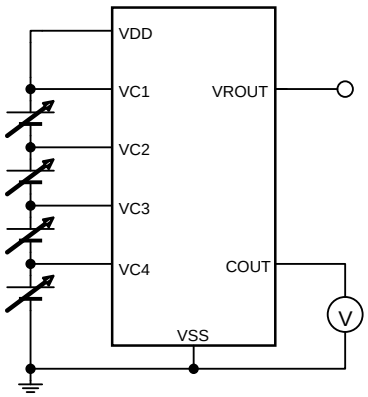

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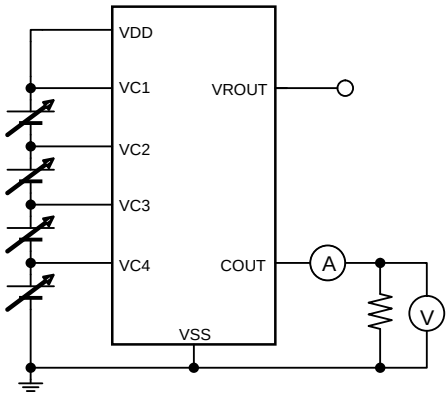

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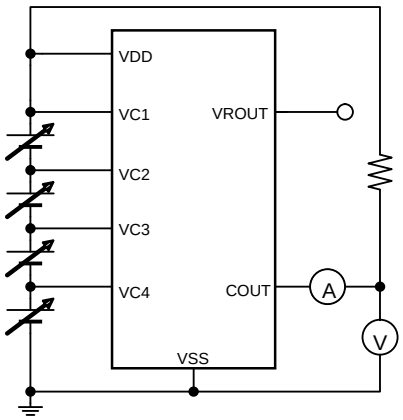

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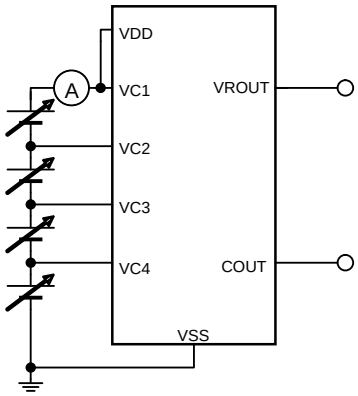
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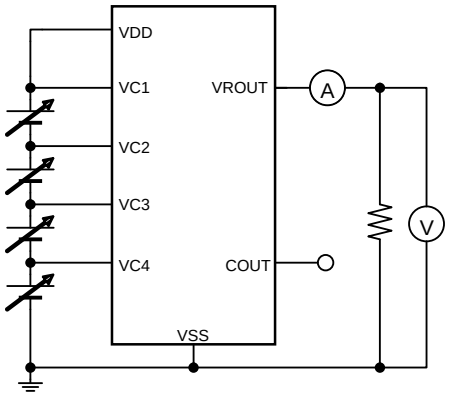
A
VC1
VROUT
VC2
VC3
VC4
COUT
VSS

H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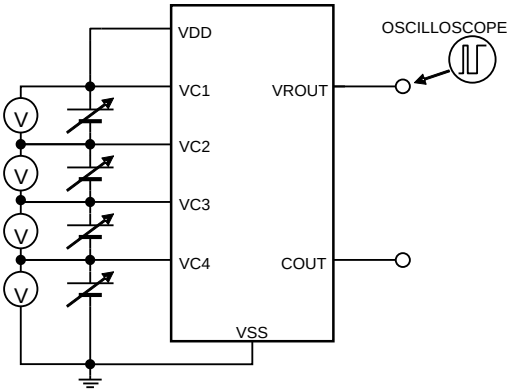
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VC4
COUT
VSS

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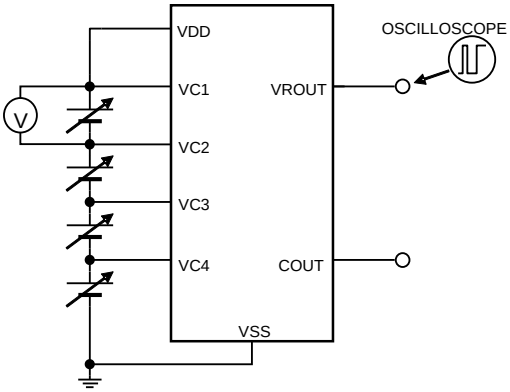
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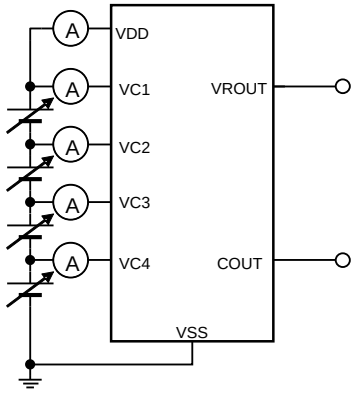
VC1
VROUT
VC2
VC3
VC4
COUT
VSS

K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VDD
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VC1
VROUT
A
VC2
A
VC3
A
VC4
COUT
VSS

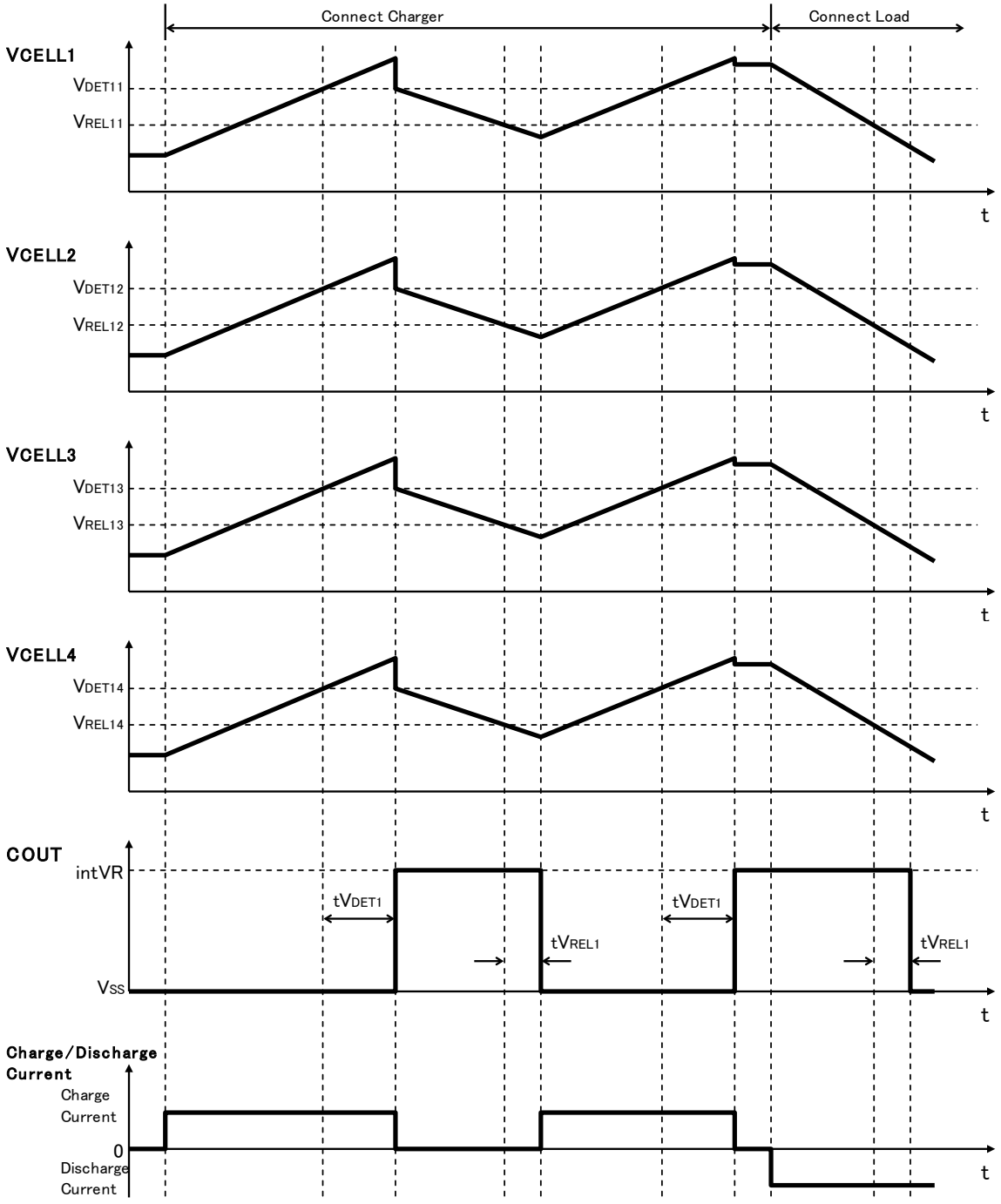
THEORY OF OPERATION

Overcharge Detection Circuit, VD1-n (n = 1, 2, 3, 4)

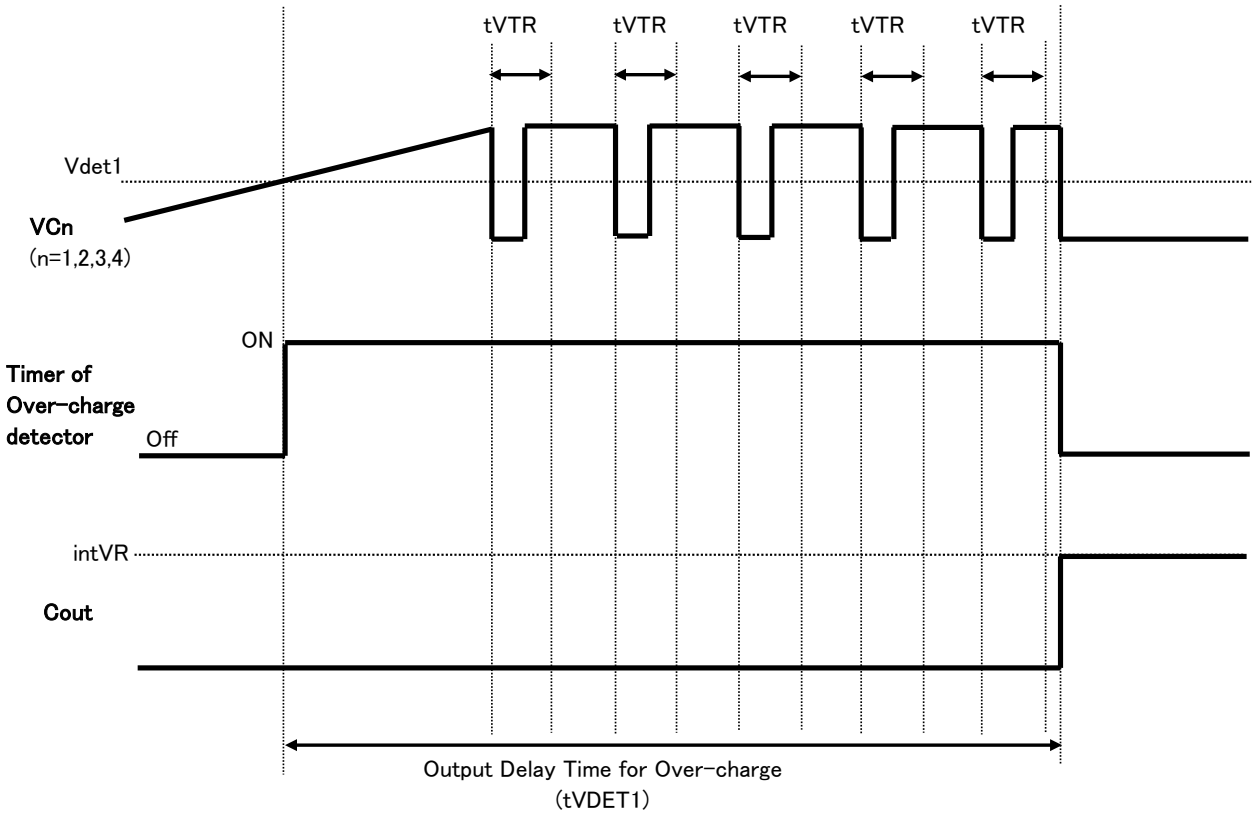
While the cells are charged, the voltage between VC1 pin and VC2 pin (Cell-1 voltage), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), and the voltage between VC3 pin and VC4 pin (Cell-3 voltage), and the voltage between VC4 pin and VSS pin (Cell-4 voltage) are supervised. If at least one of the cells' voltage becomes equal or more than the over-charge detector threshold, the over-charge is detected, and an external charge control Nch. FET turns on with COUT pin being at "H" level and by cutting a fuse on the charger path, and charge stops.

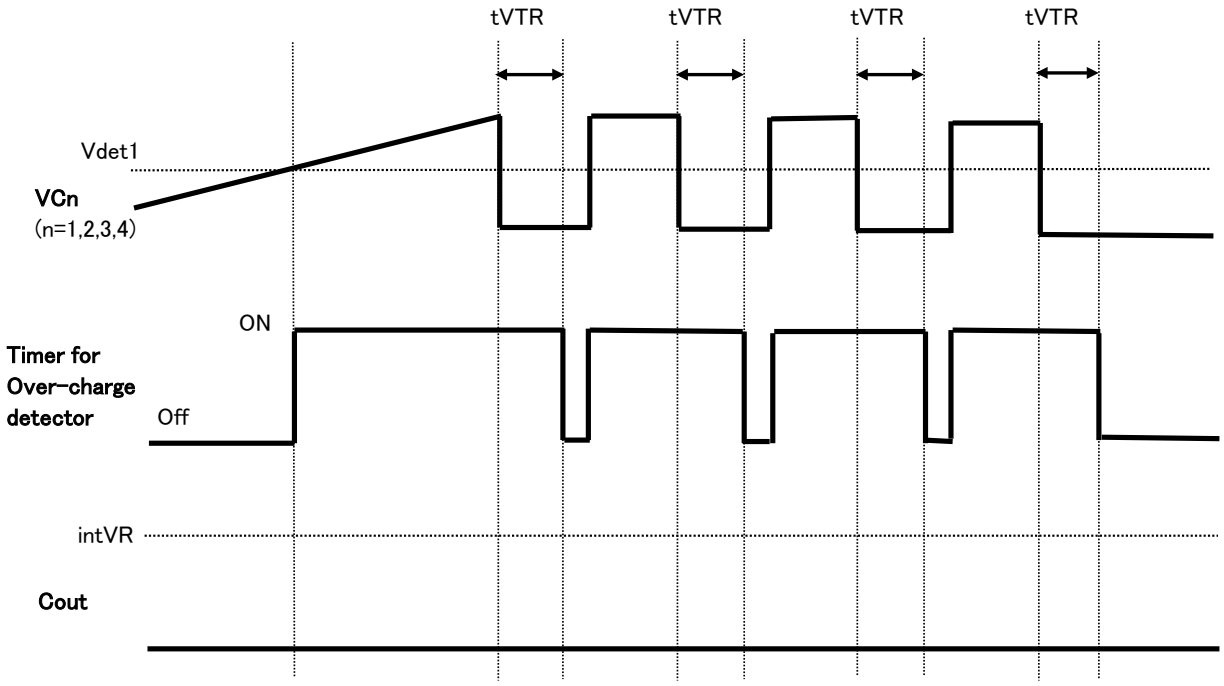
To reset the over-charge and make the COUT pin level to "L" again after detecting over-charge, in such conditions that a time when all the cells' voltages are down to a level lower than over-charge released voltage. Internal fixed output delay times for over-charge detection and release from over-charge exist. Even if one of voltage of the cells keeps its level more than the over-charge detector threshold, and output delay time passes, over-charge voltage is detected. In the case of Timer Reset Delay available version, if all the cell voltages become lower than the over-charge detector threshold within the output delay time of over-charge detector by noise or other reasons, the time period is less than over-charge detector timer reset output delay time, the over-charge delay time is accumulated and maintained, and the accumulated delay time reaches the output delay time of over-charge, the over-charge is detected. After detecting over-charge, even if all the cell voltages become equal or less than the released voltage from over-charge, if at least one of the cells voltage becomes higher than the released voltage from over-charge within the output delay time of the release from over-charge, then over-charge is not released.

The output type of the COUT pin is CMOS output between VSS and the built-in regulator, and "H" level of COUT pin is the output voltage of the built-in regulator.



Overcharge Operation Timing Chart

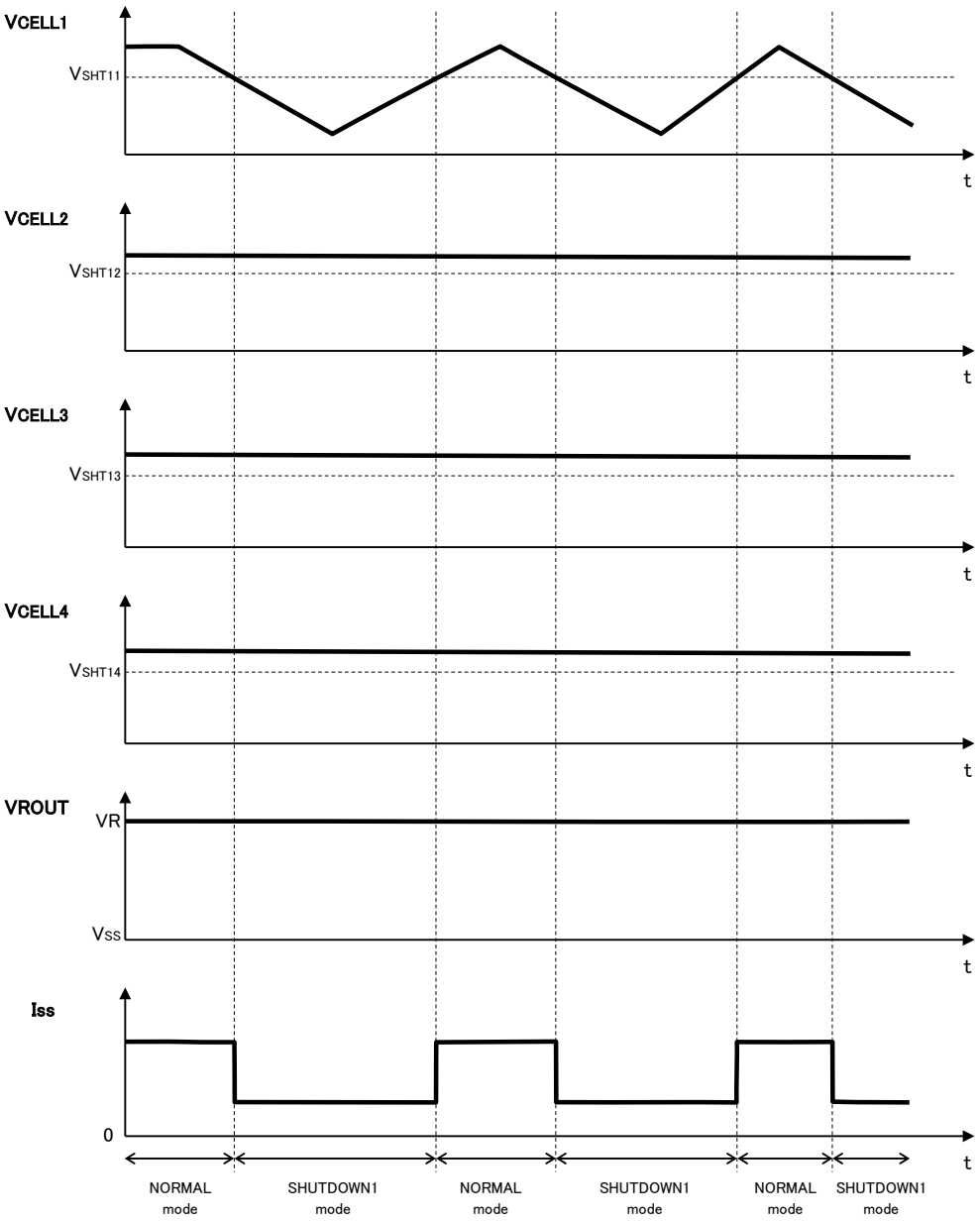




Overcharge Operation Timing Chart (Timer Reset Delay Time Function included)

Shutdown Function 1

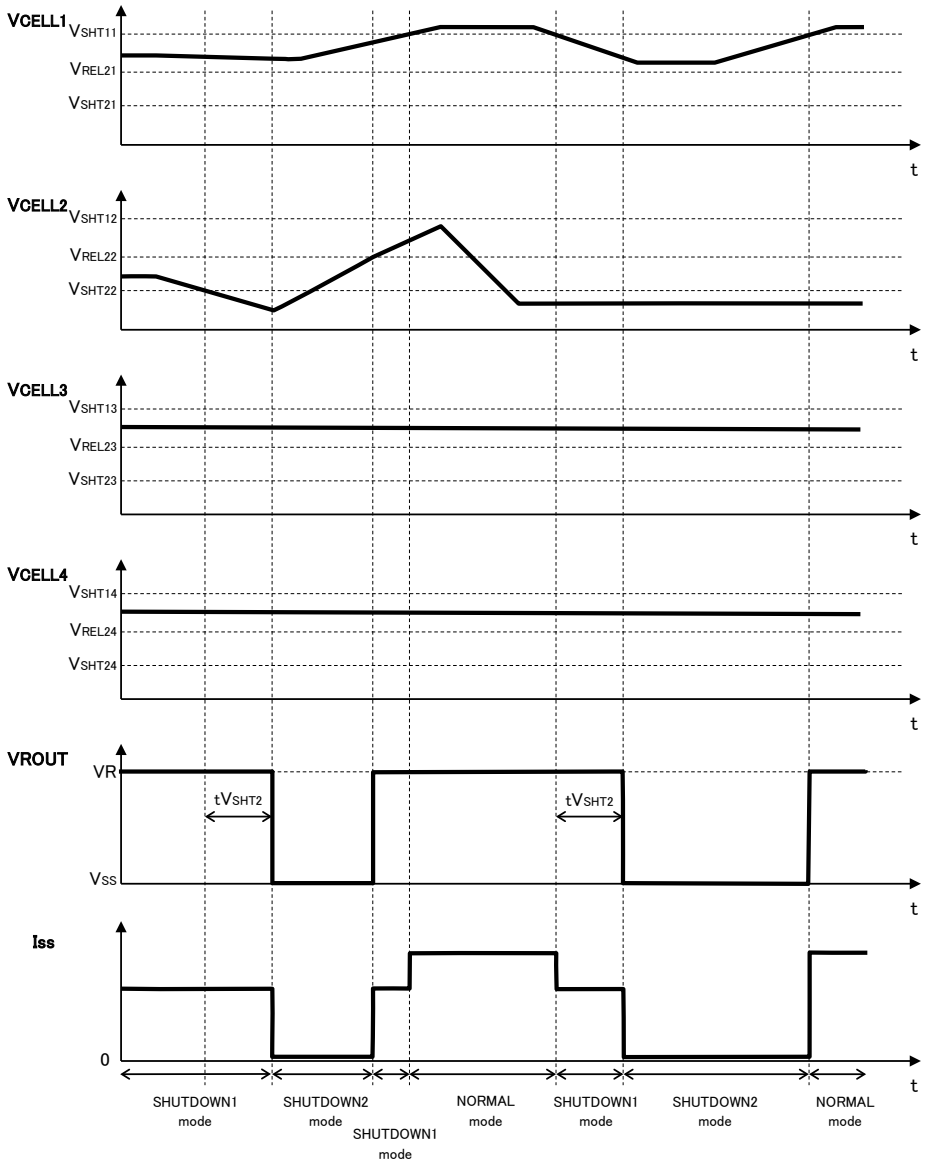
The voltage between VC1 pin and VC2 pin (Cell-1 voltage), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), the voltage between VC3 pin and VC4 pin (Cell-3 voltage), and the voltage between VC4 pin and VSS pin (Cell-4 voltage) are supervised. If the cell voltage becomes equal or less than the shutdown detector threshold1, the over-charge detector of the cell is halted, as a result, the consumption current of IC itself (Shutdown1 current) is extremely reduced. In shutdown mode1, the operation of regulator does not stop.



Shutdown Function 1 Operation Timing Chart

Shutdown Function 2

The voltage between VC1 pin and VC2 pin (Cell-1 voltage), the voltage between VC2 pin and VC3 pin (Cell-2 voltage), the voltage between VC3 pin and VC4 pin (Cell-3 voltage), and the voltage between VC4 pin and VSS pin (Cell-4 voltage) are supervised. If the cell voltage becomes equal or less than the shutdown detector threshold2 and all the cells voltages are equal or less than the shutdown detector threshold1, all the circuits are halted and shut down, as a result, the consumption current of IC itself (Shutdown2 current) is extremely reduced. In shutdown mode2, the operation of regulator stops. When all the cells voltages become higher than the shutdown2 release voltage, VR output becomes H.



Shutdown Function 2 Operation Timing Chart

Delay Shortening (DS) Function

Applying a voltage of 4 V ± 0.2 V between VDD and VC1 can shorten the overcharge detection delay time (t_{VDET1}) and the shutdown 2 detection delay time (t_{VSHT2}) into approximately 1/80, likewise, the overcharge release delay time (t_{VREL1}) into approximately 1/60.

Voltage Regulator Function

To drive the external RTC, the voltage regulator function is included in the R5439K.

2-cell/ 3-cell Protection Alternative

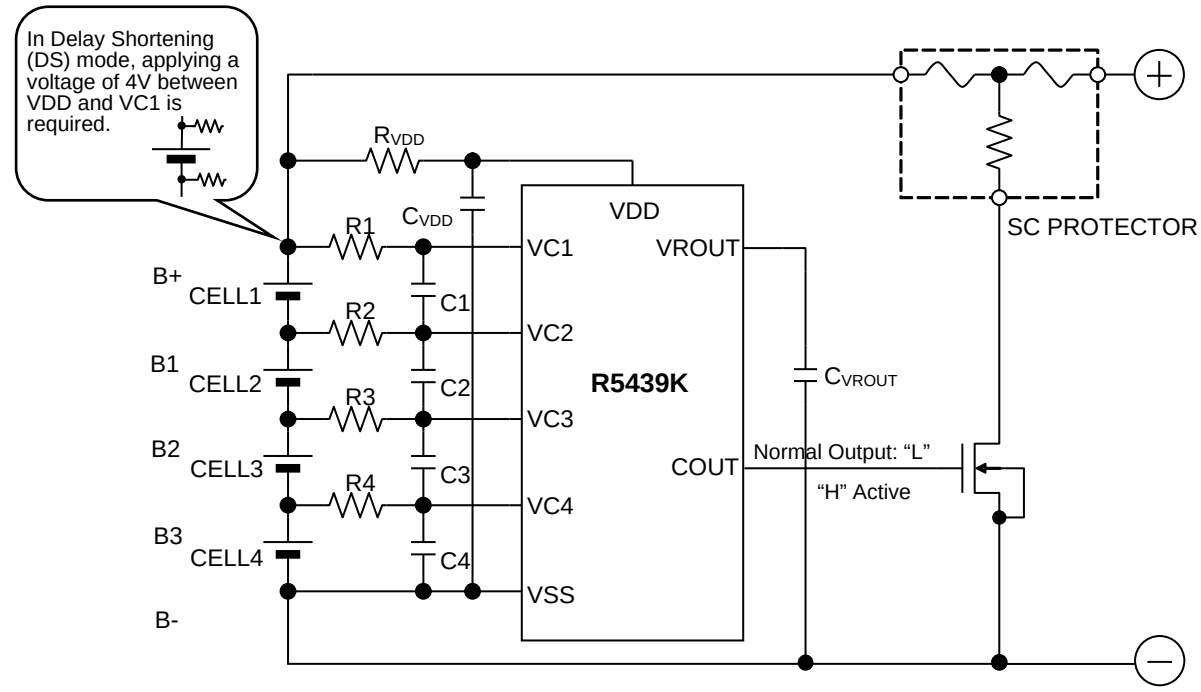
By short-circuiting between cells, the R5439K can meet as a protection IC for 2 or 3 cells placed in series. The following table indicates pins to short-circuit to VC1 depending on protected cells.

Protected Cells	Pins to short-circuit to VC1
2-cell protection	VC2 and VC3 pins
3-cell protection	VC2 pin

The 2- or 3-cell protection can only provide by the above connections.

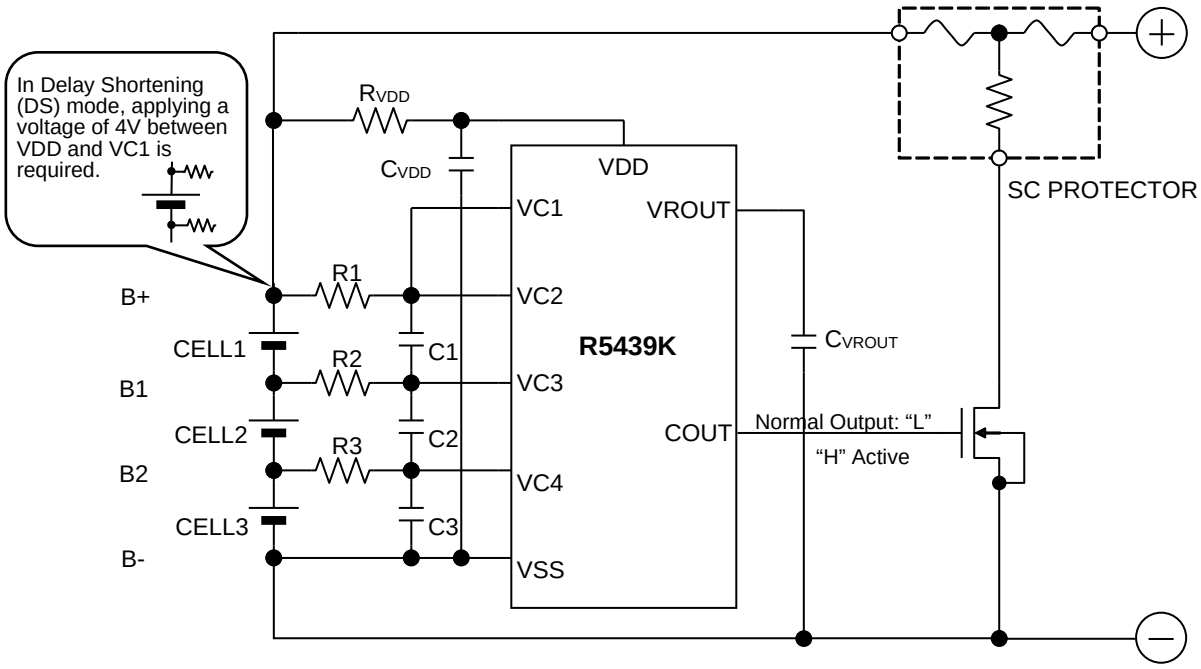
APPLICATION INFORMATION

Typical Application Circuits in Normal Mode (CMOS Output, Active-high)



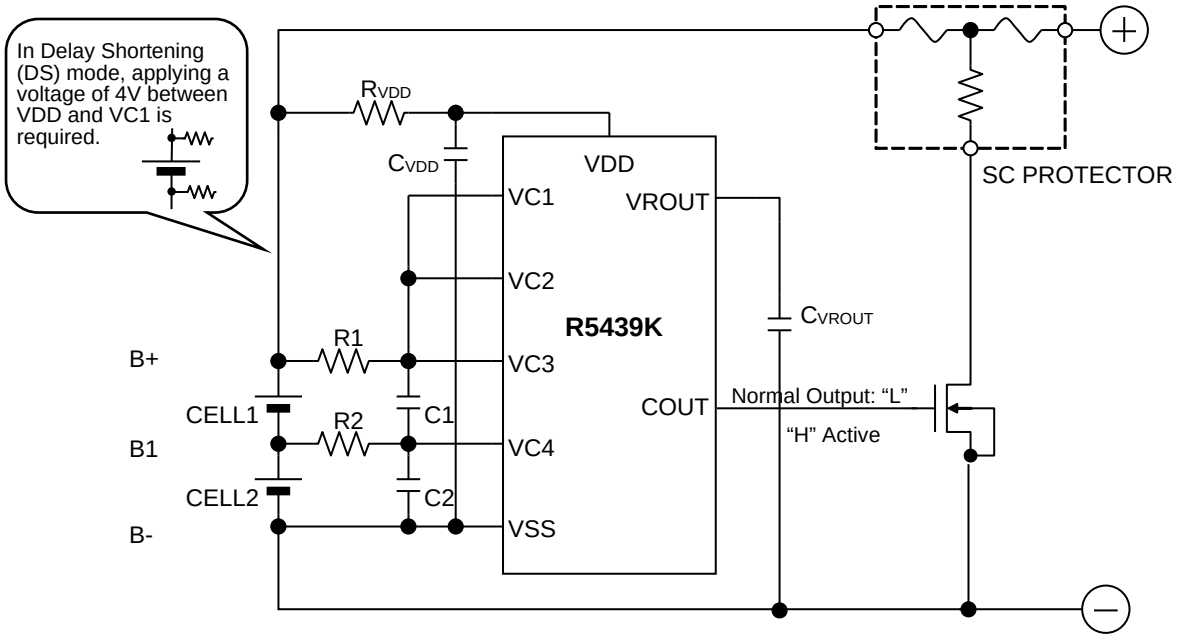
Note: Connect the pins in the following order: B-, B3, B2, B1, and B+.

4-cell Protection Circuit



Note: The 3-cell protection circuit requires to connect between VC1 and VC2. Even if shorting other pin except them, the circuit does not work as 3-cell protection. Connect the pins in the following order: B-, B2, B1, and B+.

3-cell Protection Circuit



Note: The 2-cell protection circuit requires to connect among VC1, VC2, and VC3. Even if shorting other pin except them, the circuit does not work as 2-cell protection. Connect the pins in the following order: B-, B1, and B+.

2-cell Protection Circuit

External Components

Symbol	Typ.	Unit	Range
R_{VDD}	100	Ω	100 to 1000
R1	1000	Ω	330 to 1000
R2	1000	Ω	330 to 1000
R3	1000	Ω	330 to 1000
R4	1000	Ω	330 to 1000
C_{VDD}	0.1	µF	0.01 to 1
C1	0.1	µF	0.01 to 1
C2	0.1	µF	0.01 to 1
C3	0.1	µF	0.01 to 1
C4	0.1	µF	0.01 to 1
C_{VROUT}	0.1	µF	0.1

Technical Notes on the Selection Components

- The voltage fluctuation is stabilized with R_{VDD} and C_{VDD}. If a small R_{VDD} is set, in the case of the large transient may happen to the cell voltage, by the flowing current, the IC may be unstable. If a large R_{VDD} is set, by the consumption current of the IC itself, the voltage difference between VDD pin and VC1 pin is generated, and unexpected operation may result. Therefore, the appropriate value range of R_{VDD} is from 100 Ω to 1 kΩ. The built-in voltage regulator (VR) is designed as a power source for an RTC. If the VR is used for other purpose, R_{VDD} value should be set so that V_{DD} does not become smaller than VC1-0.3V by R_{VDD} and a load current. If V_{DD} value is smaller than VC1-0.3V, the overvoltage detection voltage might shift or unexpected operation might result. To make a stable operation of the IC, the appropriate value range of C_{VDD} is from 0.01 µF to 1.0 µF.
- The voltage fluctuation is stabilized with R1 to R4 and C1 to C4. If a R1 to R4 is too large, by the conduction current at detection, the detector threshold may shift higher. Therefore, the appropriate value range of R1 to R4 is equal or less than 1 kΩ. To make a stable operation of the IC, the appropriate value range of C1 to C4 is 0.01 µF or more.
- The typical application circuit diagrams are just examples. This circuit performance largely depends on the PCB layout and external components. In the actual application, fully evaluation is necessary.
- Over-voltage and the over current beyond the absolute maximum rating should not be forced to the protection IC and external components. During the time until the fuse is open after detecting over-charge, a large current may flow through the FET. Select an FET with large enough current capacity in order to endure the large current.
- Ricoh cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Ricoh product. If technical notes are not complied with the circuit which is used Ricoh product, Ricoh is not responsible for any damages and any accidents.
- To connect the SC protector, connect the SC protector to the cell must be the last.

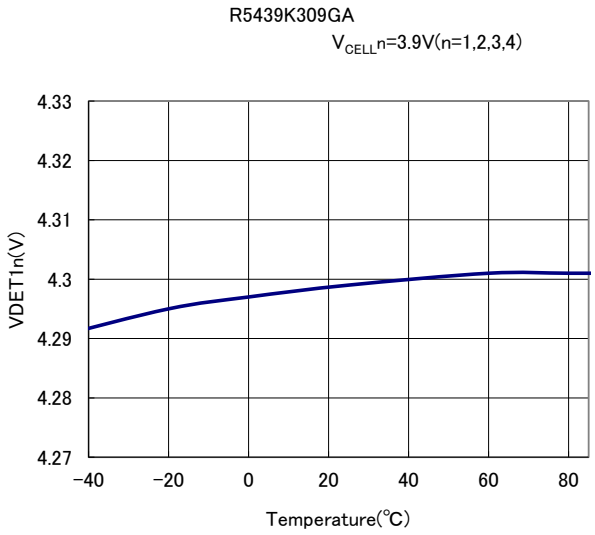
Contact Information for Inquiries regarding SC PROTECTOR

Dexerials Corporation (Sony Chemical & Information Device Company Ltd.)
Gate-city Osaki East Tower 8F, 1-11-2 Osaki, Shinagawa, Tokyo, 141-0032
TEL: 03-5435-3946
URL: http://www.dexerials.jp

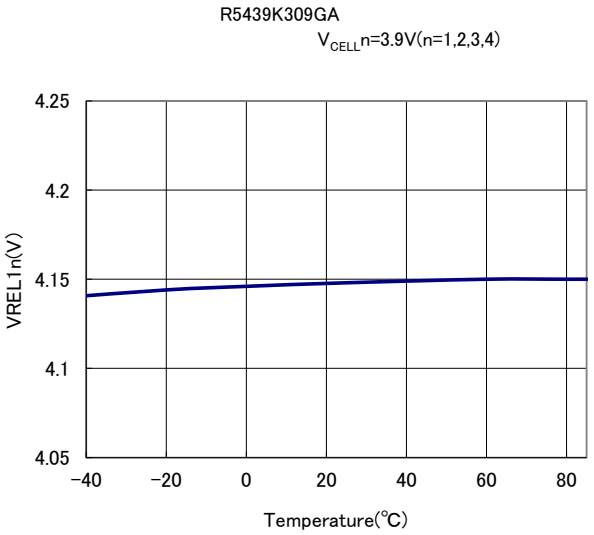
TYPICAL CHARACTERISTICS (vs. Ambient Temperature)

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

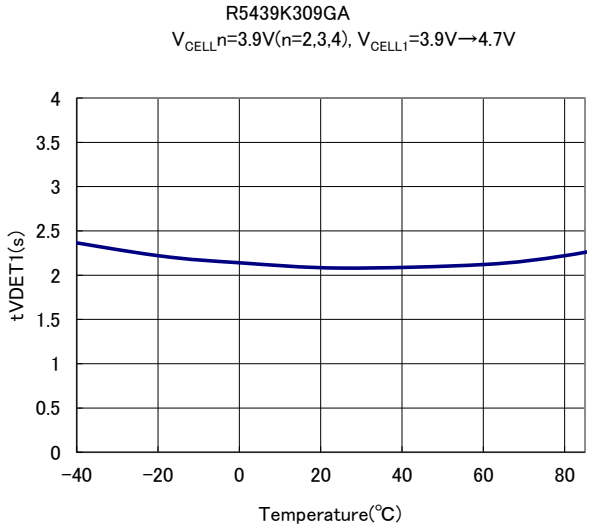
1) CELLn Overcharge Detector Threshold



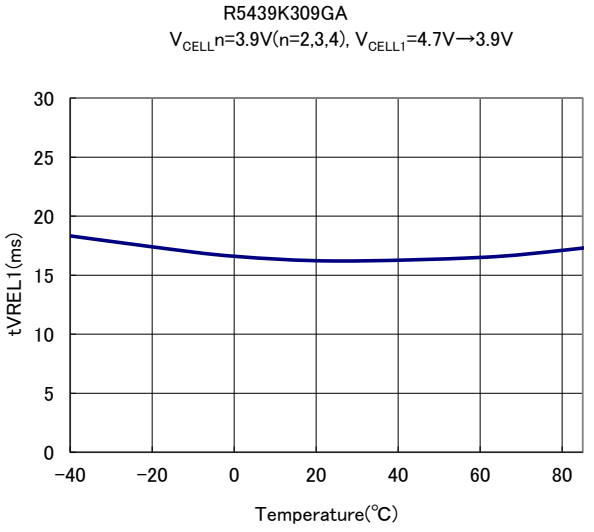
2) CELLn Overcharge Release Voltage



3) Overcharge Detection Output Delay Time



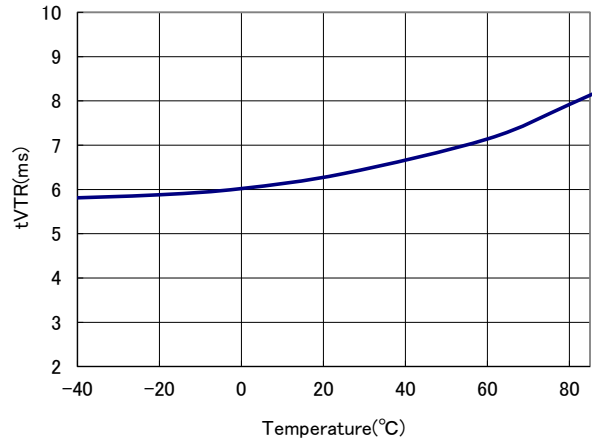
4) Overcharge Release Output Delay Time



5) Output Delay Time of Overcharge Timer Reset

R5439K309GB

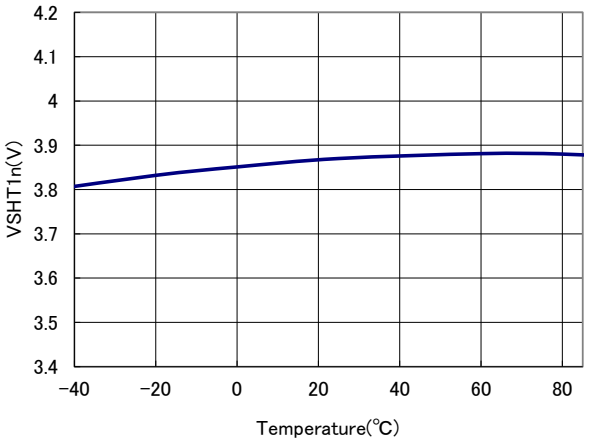
$V_{CELL}n$=3.9V(n=2,3,4), V_{CELL1}=4.4V⇔4.1V



6) CELLn Shutdown 1 Detector Threshold

R5439K309GA

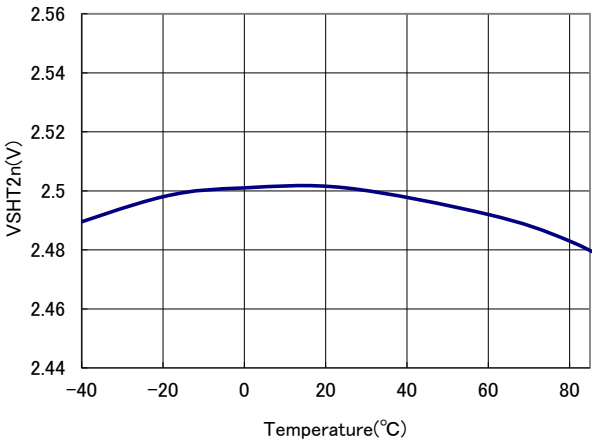
$V_{CELL}n$=3.1V(n=1,2,3,4)



7) CELLn Shutdown 2 Detector Threshold

R5439K309GA

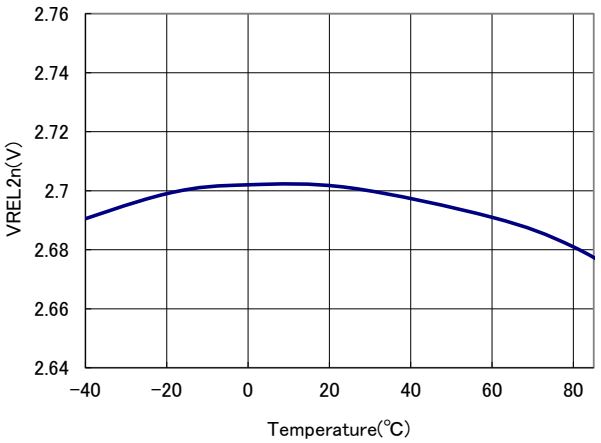
$V_{CELL}n$=3.1V(n=1,2,3,4)



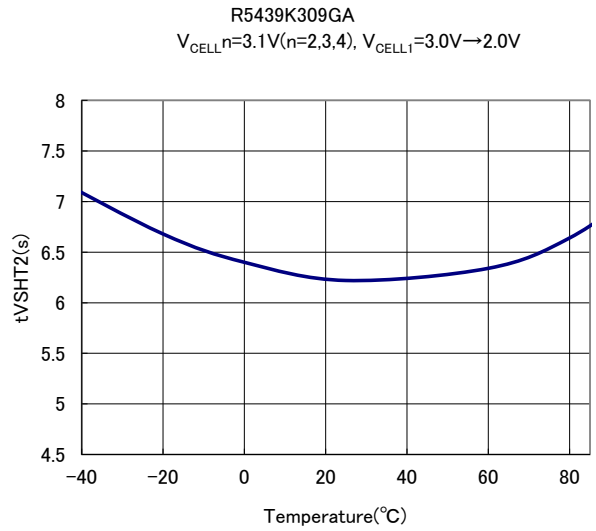
8) CELLn Shutdown 2 Release Voltage

R5439K309GA

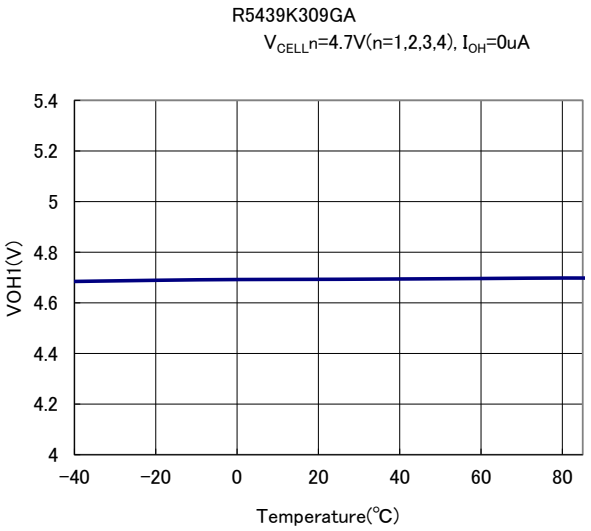
$V_{CELL}n$=3.1V(n=1,2,3,4)



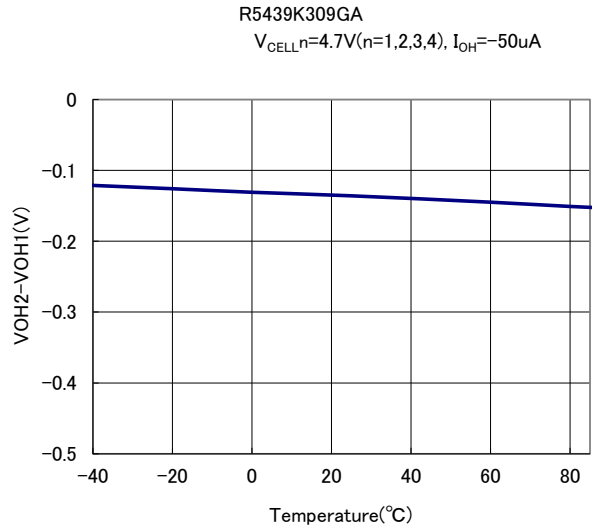
9) Shutdown 2 Output Delay Time



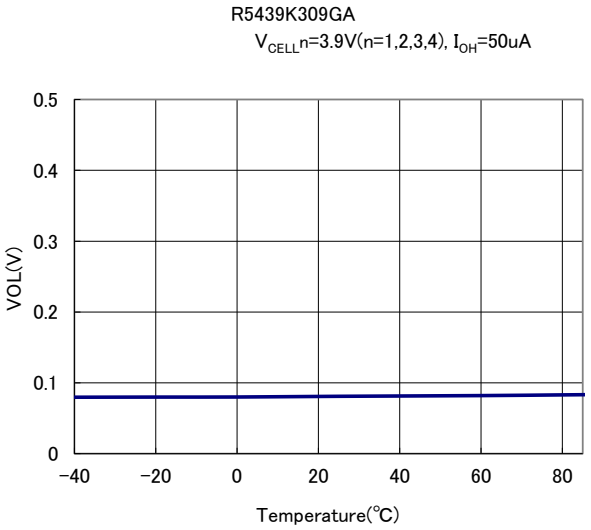
10) C_{OUT} Pch ON Voltage (No Load)



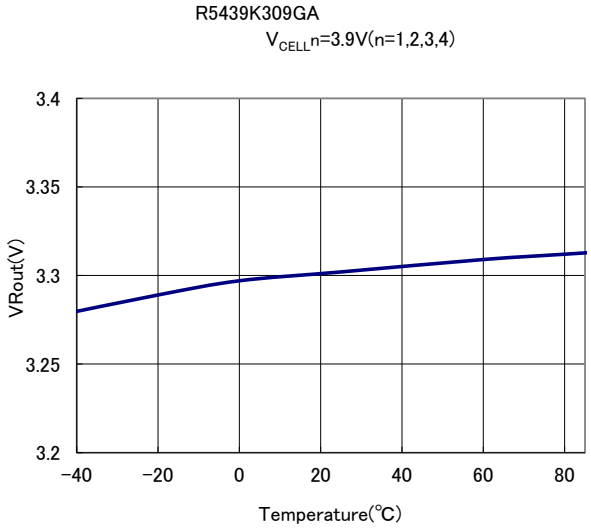
11) C_{OUT} Pch ON Voltage



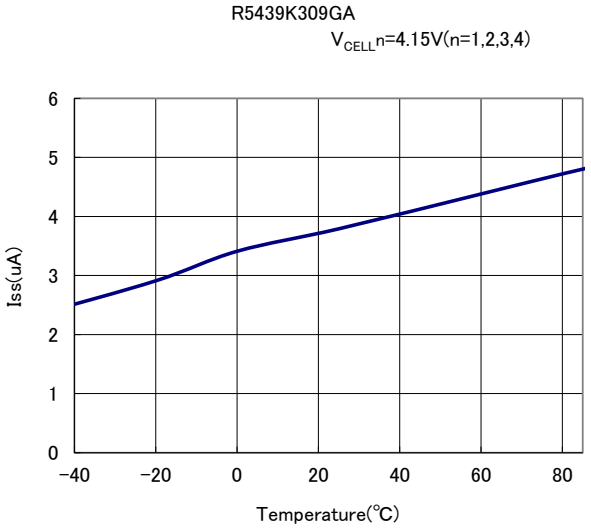
12) C_{OUT} Nch ON Voltage



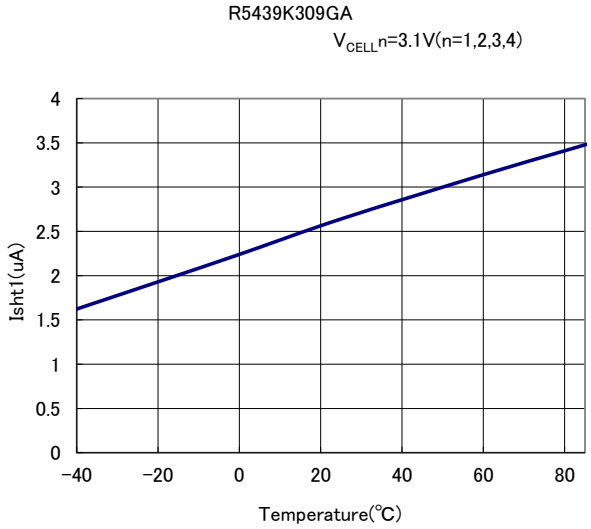
13) V_{ROUT} Output Voltage



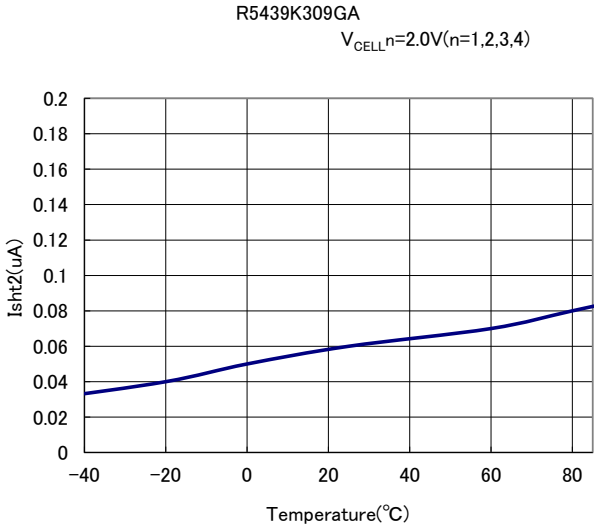
14) Supply Current



15) Shutdown 1 Current



16) Shutdown 2 Current



Ver. A

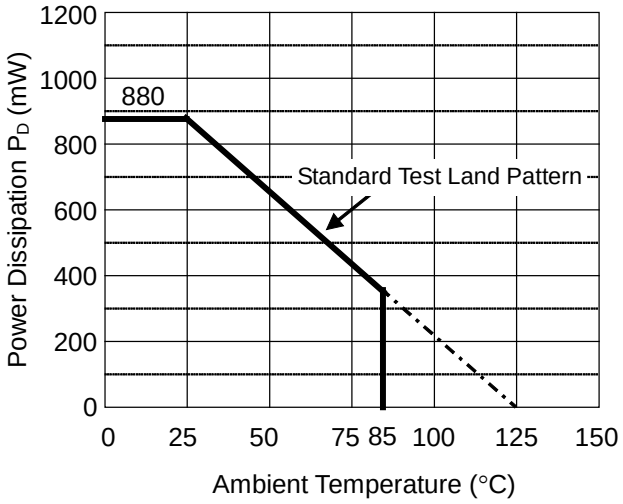
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

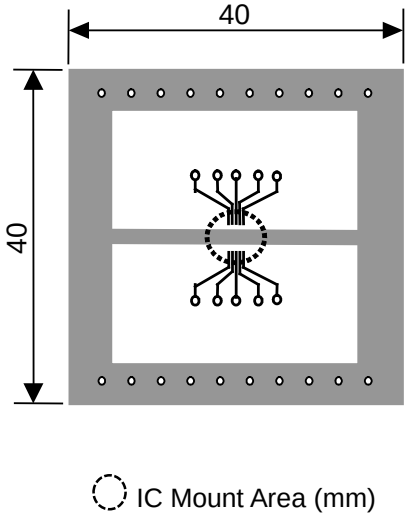
	Standard Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-Sided Board)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top Side: Approx. 50% Bottom Side: Approx. 50%
Through-holes	ϕ 0.54 mm × 30 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Test Land Pattern
Power Dissipation	880 mW
Thermal Resistance	θja = (125 − 25°C) / 0.88 W = 114°C/W

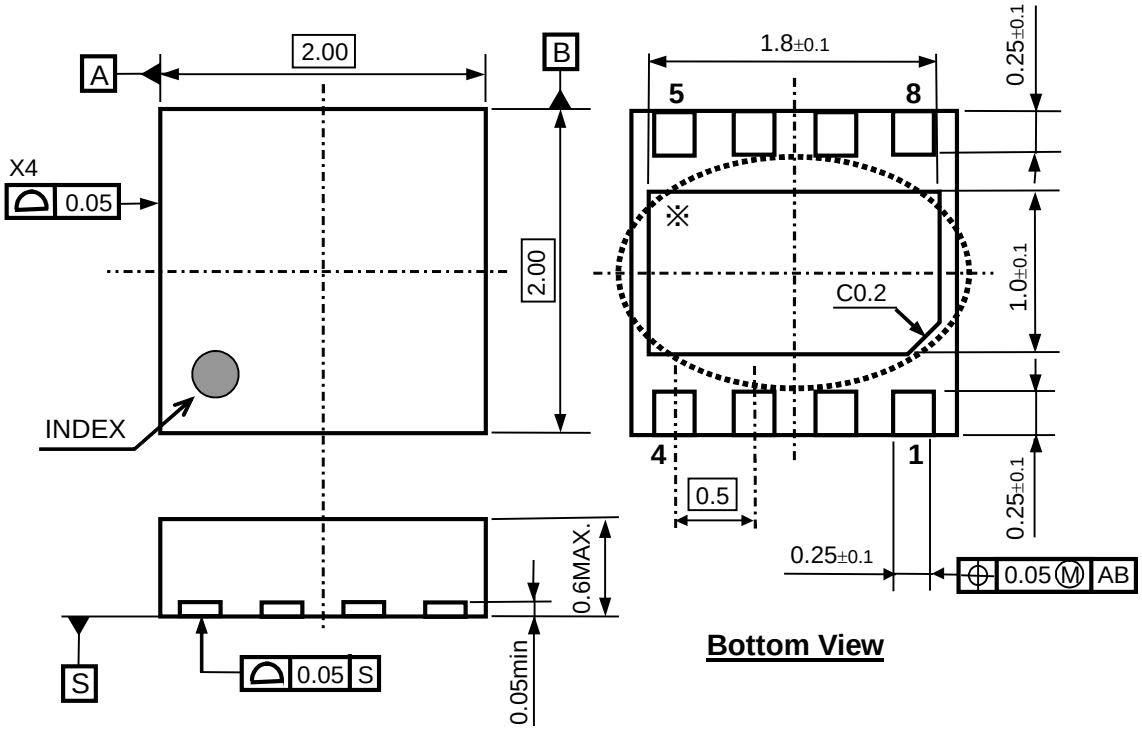


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH



DFN (PLP) 2020-8 Package Dimensions (Unit: mm)

∗ The tab on the bottom of the package is substrate level (GND). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

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Halogen Free

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