

GENERAL DESCRIPTION

The ME2307 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

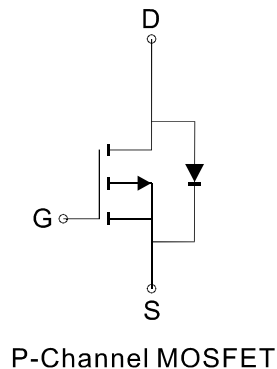
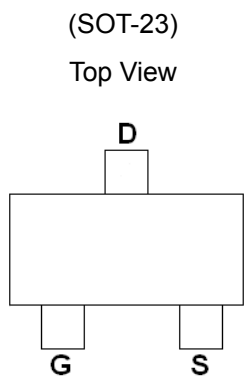
FEATURES

- $R_{DS(ON)} \leq 70m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 95m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



Ordering Information:ME2307 (Pb-free)

ME2307-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current *	I_D	$T_A = 25^\circ C$	-3.5
		$T_A = 70^\circ C$	-2.8
Pulsed Drain Current	I_{DM}	-14	A
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	1.4
		$T_A = 70^\circ C$	0.9
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	90	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper



P-Channel 30V (D-S) MOSFET

Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-10V, I _D = -3.2A		58	70	mΩ
		V _{GS} =-4.5V, I _D = -2.5A		75	95	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.8	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-1.7A		14	18	nC
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-1.7A		6.8		
Q _{gs}	Gate-Source Charge			2.8		
Q _{gd}	Gate-Drain Charge			2.3		
R _g	Gate resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		3.5	4.5	Ω
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		460	540	pF
C _{oss}	Output Capacitance			74		
C _{rss}	Reverse Transfer Capacitance			23		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-15V, R _L =15Ω R _{GEN} =6Ω, V _{GS} =-10V		33	43	ns
t _r	Turn-On Rise Time			17	22	
t _{d(off)}	Turn-Off Delay Time			39	52	
t _f	Turn-Off Fall time			5	6.5	

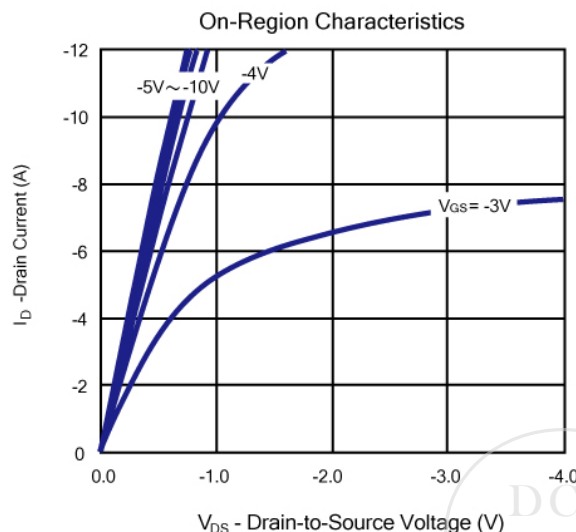
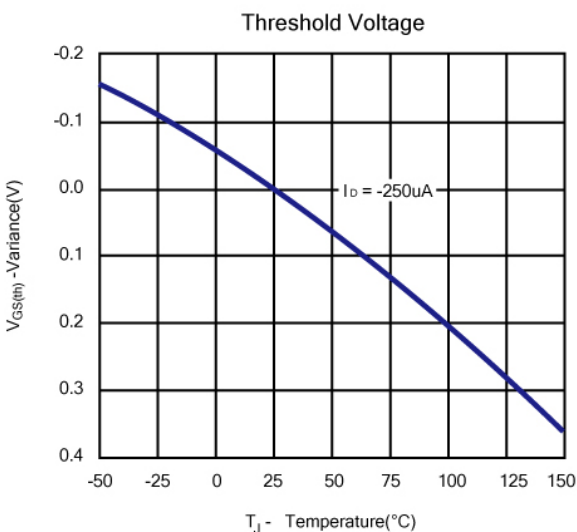
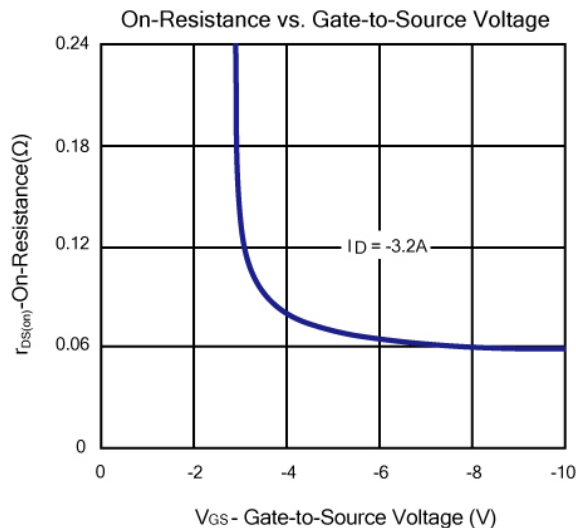
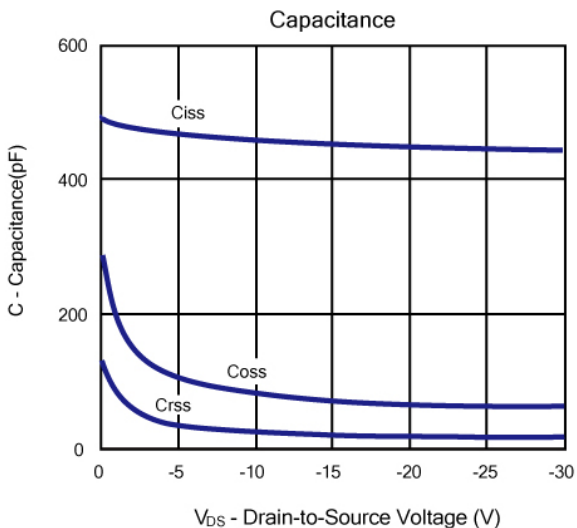
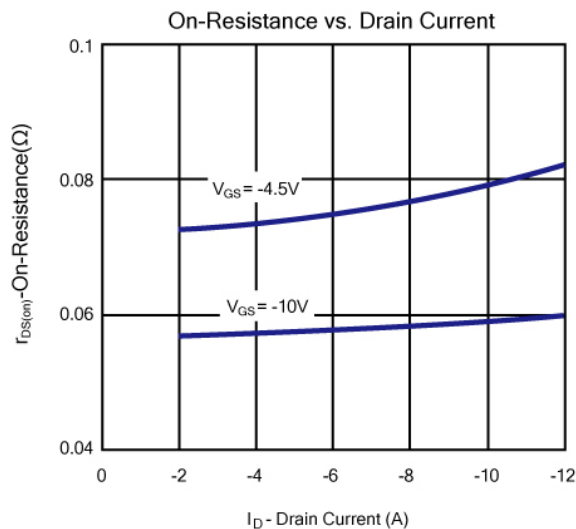
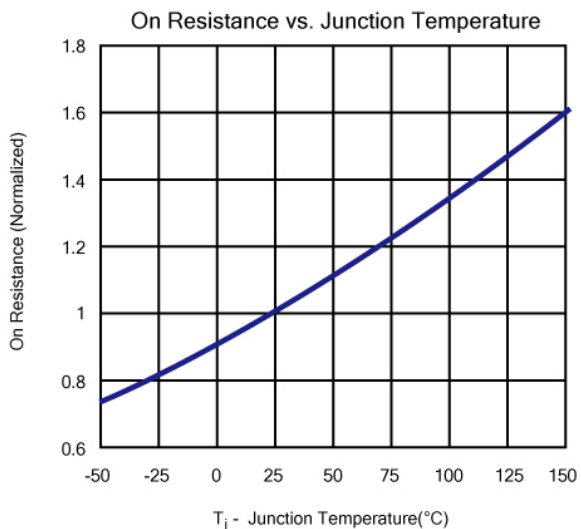
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



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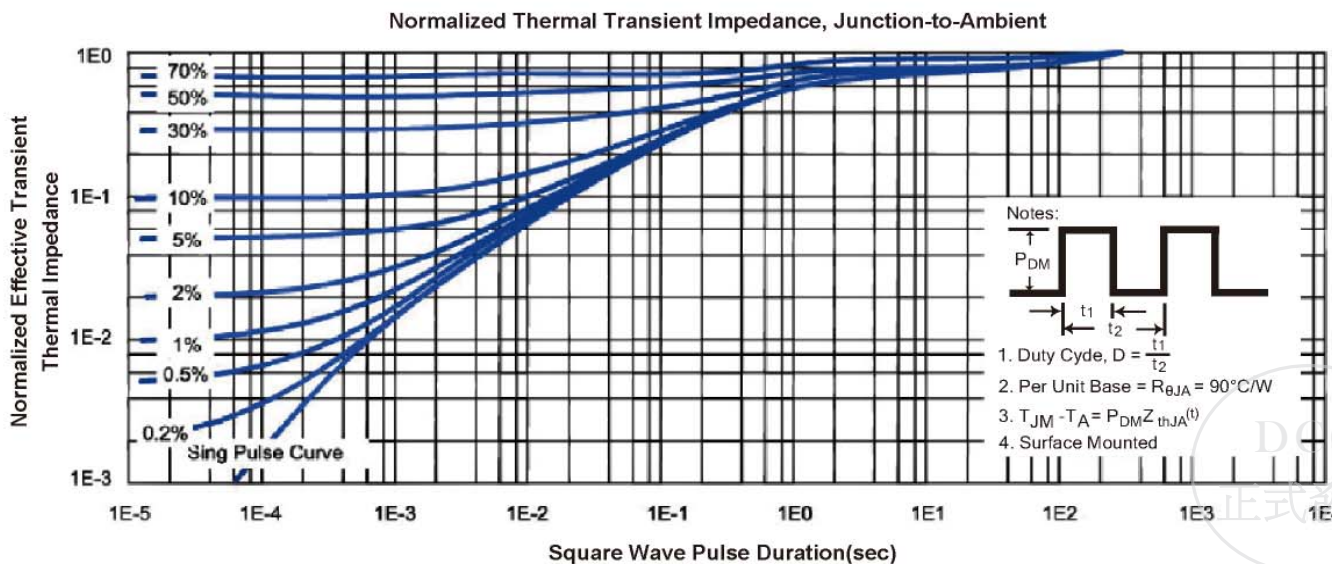
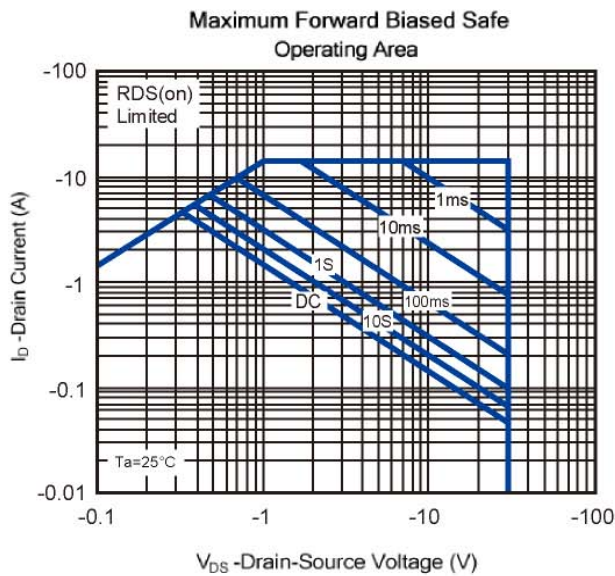
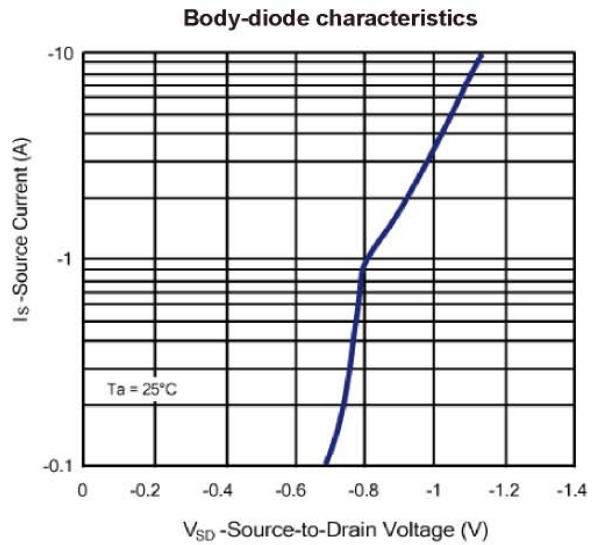
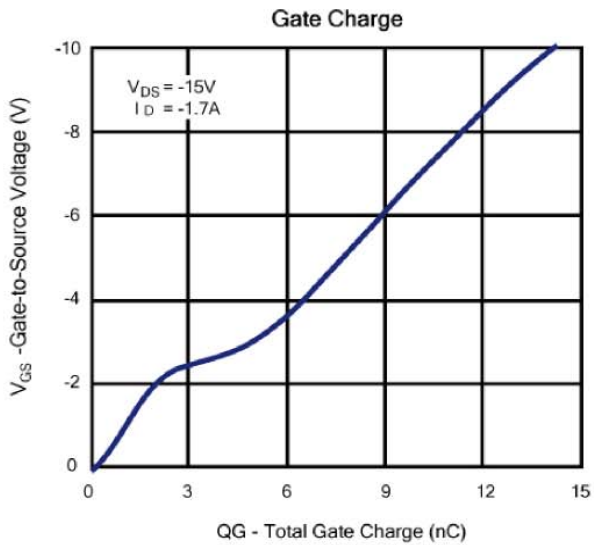
Typical Characteristics (T_J = 25°C Noted)



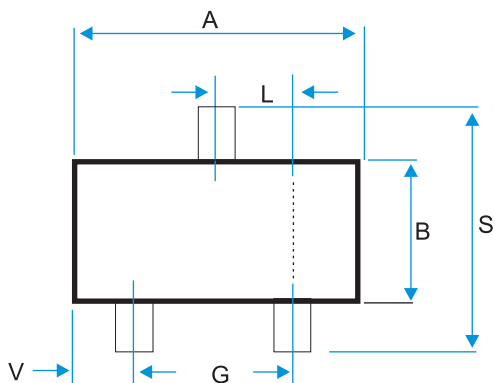
DCC
正式発行

P-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

